Figure 7-8: NAND Gates

(a) 3-input NAND gate
(b) NAND gate equivalent
(c) n-input NAND gate

Ch. 7 Text

AND-NOT

\[ \text{(d)} \quad \text{a 3-input NAND gate} \]

\[ A \implies (d) \quad (A \cdot B \cdot C)' = \]
\[ = (\text{De Morgan's Law}) = \]
\[ A' + B' + C' = \text{(from (d))} = F \]

\[ (d) \text{ is a shorthand for (c).} \]
(a) 3-input NOR gate

(b) NOR gate equivalent

(c) n-input NOR gate

Figure 7-9: NOR Gates
\( \{ \text{NAND} \} \) is a complete set of Boolean gates, i.e., this set is sufficient to realize any Boolean circuit.

We know that \( \{ \text{AND, OR, NOT} \} \) is sufficient.

NAND, as shown in the figure above, can realize NOT, AND, and OR. So, \( \{ \text{NAND} \} \) is also a complete set of Boolean gates.

An inverter built from a 3-input NAND \( (x \cdot x' \cdot x')' = x' \)
SOP realization on top
Start from SOP
\[ F = A + B'C' + B'CD \]
\[ \left[ \left[ A + B'C' + B'CD \right]^1 \right] = \left[ A' \cdot (B'C')^* \cdot (B'CD)^* \right]^1 \]
\[ \text{NAND}(B', C') \]

Figure 7-11a: Eight Basic Forms for Two-Level Circuits
Start with POS (instead of SOP)

Figure 7-11b:
Eight Basic Forms for Two-Level Circuits
Circuit 2 Discussion

\[ f = g(A, B, C, D) \]

7404 inverter (note 7405!)

\[ f(A, B, C, D) \]

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"f" indicator circuit - take it as a black box!
(1) Design a minimal SOP (AND-OR) expression for $p$ using a K-map.

(2) Design the corresponding NAND-NAND circuit.

(3) Negate the output with a 7404 inverter.

(4) The output of the 7404 inverter will be displayed using the LED indicator circuit.

(3) and (4) are on the previous page.
\[ f'(A, B, C, D) = f(A, B, C, D) = \sum m(7, 8, 9) + \sum A(10, 11, 12, 13, 14, 15) \]
The K-map for g

\[ g = A + BCD \]