Circuit 1 - continue

Design of circuits from incompletely specified functions
("don't-cares") [4.5 text]

A simple binary adder [4.6]

Full adders and their use [4.7, first part]

Karnaugh maps [5]: introduction

Daily check of 60 to 57:

60 59 58 57
Section 4.5, p. 93

(0) \( \forall x = 0: \quad F = A'B'c' + A'Bc + ABC = c' = A'B'C + BC \\
(2) \quad F = A'B'C' + A'B'c' + A'Bc + ABC = A'B'c' + BC \\
(3) \quad F = A'B'C' + A'B'c' + A'Bc + ABC' + ABC = \\
\quad = A'B' + A'Bc + AB = A'c + BC + AB = \}

N1 does not generate these configurations

Table 4-5. Truth Table with Don't Cares

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>C</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>X</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>
Design of an adder (Example 2 section 4.6)

Section 4.6, p. 95

\[ N_1 = A \quad B \]
\[ N_2 = C \quad D \]
\[ N_3 = X \quad Y \quad Z \]

**Truth Table:**

<table>
<thead>
<tr>
<th>( N_1 )</th>
<th>( N_2 )</th>
<th>( N_3 )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \overline{A} \overline{B} )</td>
<td>( \overline{C} \overline{D} )</td>
<td>( \overline{X} \overline{Y} \overline{Z} )</td>
</tr>
<tr>
<td>0 0</td>
<td>0 0</td>
<td>1 0 0 0 0 0</td>
</tr>
<tr>
<td>0 0</td>
<td>0 1</td>
<td>0 0 0 1 0 1</td>
</tr>
<tr>
<td>0 0</td>
<td>1 0</td>
<td>1 0 1 0 1 0</td>
</tr>
<tr>
<td>0 0</td>
<td>1 1</td>
<td>1 1 0 1 1 0 0</td>
</tr>
<tr>
<td>0 1</td>
<td>0 0</td>
<td>1 1 0 0 1 1</td>
</tr>
<tr>
<td>0 1</td>
<td>0 1</td>
<td>1 1 0 0 1 1</td>
</tr>
<tr>
<td>0 1</td>
<td>1 0</td>
<td>1 1 0 0 1 1</td>
</tr>
<tr>
<td>0 1</td>
<td>1 1</td>
<td>1 1 0 0 1 1</td>
</tr>
</tbody>
</table>

**Section 4.6, p. 95**

\[ E \quad 8 \quad N_1 = A \quad B \quad C \quad D \quad X \quad Y \quad Z \]
\[ N_3 = \sum m(7,10,11,13,14,15) \]
\[ Y(A,B,C,D) = \sum m(2,3,5,6,8,9,12,15) \]
\[ Z(A,B,C,D) = \sum m(1,3,4,6,9,11,12,14) \]
Design of Binary Adders (4.7)

Add two 4-bit unsigned numbers, giving a 4-bit number as result. Also, allow a 1-bit carry as input and a one-bit carry as output.

\[
\begin{align*}
C_4 &+ A_3 A_2 A_1 A_0 \\
+ B_3 B_2 B_1 B_0 &
\end{align*}
\]

\[C_4 S_3 S_2 S_1 S_0\]

Figure 4-2: Parallel Adder for 4-Bit Binary Numbers

This circuit has nine inputs — too big!
Instead, connect four full adders.

\[
\begin{align*}
1011 & = A_3 A_2 A_1 A_0 \\
+ 1011 & = B_3 B_2 B_1 B_0 \\
\hline
\overbrace{1010} & = \underbrace{S_3 S_2 S_1 S_0}
\end{align*}
\]

Figure 4-3: Parallel Adder Composed of Four Full Adders

Each full adder adds two one-bit numbers and a carry, and produce one one-bit number and a carry.
\[
\text{Sum} = \sum m(1, 2, 4, 8) = \\
= x' \cdot y' \cdot c_{in} + x' \cdot y \cdot c_{in}' + x \cdot y' \cdot c_{in}' + x \cdot y \cdot c_{in} = \\
= x' \cdot (y' \cdot c_{in} + y \cdot c_{in}') + x \cdot (y' \cdot c_{in} + y \cdot c_{in}) = \\
= x' \cdot (y' \oplus c_{in}) + x \cdot (y \oplus c_{in}) = \\
= x' \cdot (y' \oplus c_{in}) + x \cdot (y \oplus c_{in})' = \\
= x \oplus (y \oplus c_{in}) = \left[3 \text{ or } 13\right] \text{: associativity}
\]

of exclusive-or (\(\oplus\)) = \(x \oplus y \oplus c_{in}\)

\[
\text{Cout} = \sum m(3, 5, 6, 7) = x' \cdot y \cdot c_{in} + x \cdot y' \cdot c_{in} + x \cdot y \cdot c_{in}' + x \cdot y' \cdot c_{in}' = \\
= (x' \cdot y \cdot c_{in} + x \cdot y' \cdot c_{in}) + (x \cdot y' \cdot c_{in} + x \cdot y' \cdot c_{in}) + (x \cdot y \cdot c_{in} + x \cdot y \cdot c_{in}) = \\
= y \cdot c_{in} + x \cdot c_{in} + x \cdot y
\]
Here are the resulting circuits:

Figure 4-5: Implementation of Full Adder
A Karnaugh map for two variables (A and B)

Section 5.2, p. 121
<table>
<thead>
<tr>
<th></th>
<th>A</th>
<th>B</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Figure 5-1a, b, c, and d