CSCE 211H **Test 2** **Nov 20**

1. Carry Lookahead
   (a) In designing a 6 bit carry look ahead unit, give the formula for G_{block}.
   (b) Draw a Block Diagram for a 3 Bit Carry lookahead unit (3CLU)
   (c) Give the VHDL behavioral section for a VHDL module for a three bit CLU. build an 18 bit carry lookahead adder.
   (d) What is the propagational delay for this adder?
   (e) If we were to add one more level of carry-look-ahead unit whatt would be the maxiumum size adder that we could implement? and what is the propagational delay for this adder?
2. Design a 4 bit register that will perform a parallel load and a two's complement using control lines L(load) and C(complement). The control lines should be passed through circuitry that will ensure that if both L=1 and C=1 then neither operation is performed.
3. Sequential Design Problem:

   If C is a clock signal with period 10 seconds, i.e, 5 seconds C=0, then for 5 seconds C=1 and this repeats forever.

   Use this signal C to specify transitions for a traffic light controller. For the EW light there should be 20 seconds of green, 5 seconds left turn only, 5 seconds yellow, then red for 30 seconds. If for the NS we have no left turn signal what should the NS lights be corresponding to to the EW assuming no overlap of red. (Of course this is ridiculous but it makes this design simpler.) Assume also that there is a sensor (signal S) that measures whether there is any NS traffic. If there is no NS traffic the green should be extended by ten second intervals until there is NS traffic.

   So the inputs we have are C and S. Draw the state diagram.
4. Given the state diagram below generate the corresponding state table.
5. (a) Give the excitation table for an RS flip-flop.
   (b) Convert the state table below to an excitation table with flip-flop inputs assuming that flip flop A is a RS flip flop and flip-flop B is a D flip-flop.
6. Xilinx:
   (a) Explain the process you would go through to simulate a VHDL design created using Xilinx using ModelSim.
   (b) For the digilab boards how does establish connections between an I/O marker say "A" and connect it to say "Switch 1" on the board assuming that you know that pin "P57" connects to this switch.