1. (15) Bases
   (a) Convert 782_{10} to hex
   (b) Convert $.782_{10}$ to hex (at most three digits)
   (c) Convert $1A2.12_{16}$ to decimal (at most three decimal places)
   (d) Convert 1110111.11001 to hexadecimal
2. (a) compute the Dual of $X \cdot (Y + Z) = X \cdot Y + X \cdot Z$
   (b) Identify Figure A from the figure sheet.
   (c) Identify Figure C from the figure sheet.
   (d) Identify Figure D from the figure sheet.
   (e) What is the propagational delay for the circuit shown in Figure B?
3. (15) Integers representations (use 8 bits except for e)
   (a) Represent 70 as an 8 bit unsigned integer
   (b) Represent 70 as an 8 bit signed-magnitude integer
   (c) Represent -70 as an 8 bit signed-magnitude integer
   (d) Represent 70 as an 8 bit two's complement integer
   (e) Represent -70 as an 8 bit two's complement integer
4. (15) Minimization
   (a) What is a prime implicant?
   (b) What is an essential implicant?
   (c) Simplify in Sums of Products form: $F(X, Y, Z) = \sum m(0, 1, 4, 5, 7)$
5. (15) Minimization II
   (a) Simplify $F(W, X, Y, Z) = \sum m(1, 3, 5, 6, 7, 9, 11)$
   with don't care conditions $d(W, X, Y, Z) = \sum m(4, 8, 10)$.
   (b) Simplify the same function in Products of Sums form.
6. Show how to construct a 32-to-1 line multiplexer from five 8-to-1 line multiplexers. One will not be fully utilized.
7. Analyze the CMOS Circuit in figure E
8. Construct a quad 5-to-1-line multiplexer with four single 4-to-1-line multiplexers and one quadruple 2-to-1-line multiplexer.
9. VHDL
   (a) What does the entity section of a VHDL description specify?
   (b) In Structural VHDL specifications what statement is used to hook-up components?
   (c) Give the portion of the architecture section of seven segment display driver that generates segment "a."