1. (15) Bases

2. Short answer
   (a) Compute an even parity-bit for 1110100
   (b) \((X + Y + Z) = \)
   (c) Distributive Laws:
       \(X \cdot (Y + Z) = \)
       \(X + YZ = \)
   (d) What is the propogational delay for a 10 bit ripple carry adder?
   (e) Express \(8_{10}\) in excess-3

3. (15) Identify the following Circuits:
   (a) 2-to-4 decoder figure 3-24
   (b) 4-to-1 Mux figure 3-19
   (c) Priority Encoder
   (d) CMOS inverter

4. (15) Minimization
   (a) Identify the prime implicants and the essential implicants.
   (b) Simplify in Sums of Products form:
       \(F(X, Y, Z) = \sum m(0, 2, 5, 6, 7)\)
   (c) Show how to implement \(F(A, B, C) = AB + AC + BC\) using NAND gates

5. (15)
   (a) Simplify \(F(W, X, Y, Z) = \sum m(0, 1, 4, 5, 7, 10, 14, 15)\)
       with don't care conditions \(d(W, X, Y, Z) = \sum m(2, 6, 9, 11, 13)\).
   (b) Simplify in Products of Sums form:

6. Show how to construct a 16-to-1 line multiplexer from five 4-to-1 line multiplexers

7. Analyze the CMOS Circuit

8. Construct a quad 9-to-1-line multiplexer with four single 8-to-1-line multiplexers and one quadruple 2-to-1-line multiplexer. The multiplexers should be interconnected and inputs labeled so that the selection codes 0000 through 1000 can be directly applied without added logic.

9. Test 2

10. Since Test 2
    - Memory
    - Block diagrams etc
    - VHDL / Xilinx
    - PLA, PALs, ROMS