CSCE 211H **Exam Dec 9**

1. Represent the following numbers in the following forms using 12 bits:
   - 777_{10}
   - -777 in signed magnitude
   - -777 in two's complement
2. Analyze the CMOS Circuit
3. Simplify $F(W, X, Y, Z) = \sum m(0, 2, 4, 9, 11)$
   with don't care conditions $d(W, X, Y, Z) = \sum m(1, 5, 6, 9, 10, 13, 15)$.
4. Sequential Design Problem: Design a state machine controller for a automatic toll both that raises an arm after $.45 or more in quarters, and dimes (no nickels, or pennies allowed) have been inserted. No change is given.
5. Construct the state table for this problem.
6. Describe in detail the remaining steps in constructing the circuitry for the toll change booth controller.
7. Show the construction of a 4-bit register that will allow parallel load and also can perform a two's complement. Each control (L and C) should turn the other off.
8. Give a behavioral section for a VHDL module for the block generate and block propagate of a 4 bit CLA unit.
9. Describe the constrcution of static and dynamic RAM memory cells. Give a block diagram of a 64K x 8 RAM listing all inputs, giving the number of address and data lines. Using 64K x 8 units and a decoder show how to construct a 256K x 32 RAM.
10. Lab Question: Design a 4 bit counter with a carry. Hook six of these in series to make a 24 bit counter. This counter should have a reset, and an enable and 4 parallel outputs. The 4-bit counter can include a parallel load capability, **but you should not try to supply 24 inputs to the 24-bit counter.** That is the 24 bit counter should not have a parallel load capability. You should implement this with the Xilinx software and using a seven segment driver download this onto the digilab board and drive the first digit of the seven segment display.