Photonic Packaging for Mixed-Technology Sensor Systems

Donald Chiarulli, Jason Bakos, and Leo Selavo
Department of Computer Science, Room 6135 Sennott Square Bldg,
University of Pittsburgh, Pittsburgh PA 15260
don@cs.pitt,edu *jbakos@cs.pitt.edu* *elo@cs.pitt.edu*

Steven Levitan
Department of Electrical Engineering, Room 348, Benedum Hall,
University of Pittsburgh, Pittsburgh, PA 15261
steve@ee.pitt.edu

John Hansson and Michael Weisser
Schott Fiber Optics, 122 Charlton Street
Southbridge, MA 01550

Abstract

Densely integrated systems in the future will incorporate device and communication technologies that span optics, electronics, micro-mechanics, and micro-fluidics. Given the fundamental differences in substrate materials, feature scale and processing requirements between integrated devices in these domains, multi-chip, system-in-package (SIP) designs will be required. In this paper we present our research on a multi-technology volumetric substrate for these packages that can transport optical signals interleaved in the same volume with electrical signals, micro-fluidic channels and power and ground planes.

Summary

Photonics technology is rapidly expanding into a new generation of systems that are enabled by the dense co-integration of optoelectronic elements and advanced sensing. Among the sensing mechanisms at the core of these systems are photonic MEMs, biophotonic interactions, spectroscopic analysis, chemical florescence and chromatography. The implementation and packaging of these systems is a particularly difficult problem since they incorporate devices that span electronics, optics, micro-mechanics, and micro-fluidics. There are fundamental differences in substrate materials, feature scale and processing requirements between integrated devices in these domains. It is likely that multi-chip, system-in-package (SIP), integration solutions will be required for the foreseeable future. In this paper we discuss our current research into photonic packaging for multi-chip/multi-technology systems. Our focus is on the development of a heterogeneous substrate capable of transporting electrical signals, power and ground in the same volume as a optical signals and fluidic materials.

The starting point for this research is our current research into optical interconnections within CMOS/optoelectronic multi-chip-modules (OEMCMs). Our research group has already demonstrated volumetric OE-MCMs [1,2,3,4] based on guided image transport through fiber image guides (FIGs). We have built and demonstrated centimeter scale volumetric solids designed to transport arrays of optical channels between chips mounted the outside surfaces. The goal of our current work is extend the OE-MCM designs to support larger and more complex CMOS devices and to support the integration of complex CMOS with photonic sensors based on MEMs or micro-fluidic devices. This requires a mechanism for interleaving optical transport with electrical interconnections, micro-fluidic channels and electrical power and ground planes across each surface of each device. To provide these capabilities, we exploit the fact that the same manufacturing process for FIGs can also produce dense arrays of capillaries. By integrating capillaries into the optical transport media we can provide both fluidic transport between micro-

fluidic devices or for fluidic I/O and, by depositing electrical conductors into these capillaries, we can provide a conduit for low bandwidth, point-to-point electronic signals.

A conceptual drawing of one such package is shown in Figure 1. In this design, a mixture of micro-fluidic, and analog and digital electronic components are mounted on the outside surfaces of a polyhedral solid. The solid is made from stacked layers of capillary/image guide material. Each layer is cut with a different angular bias and oriented to connect a pair of surfaces. By incorporating metal planes between the stack layers electrical power and ground can be included. Input and output for the package uses polyhedron surfaces that are not populated by chips and thermal extraction paths are implemented though heat sinks (not shown in the figure) in contact with the bottom side of each chip and/or by directly cooling the solid itself. Figure 2 shows a sample of our EO-chip technology based on Silicon-on-Sapphire will full area electrical I/O. Figure 3 shows samples of FIG material configured with optical fibers and showing a sample SoS chip on the top surface. Figure 4 is and capillary arrays fabricated using FIG technology.

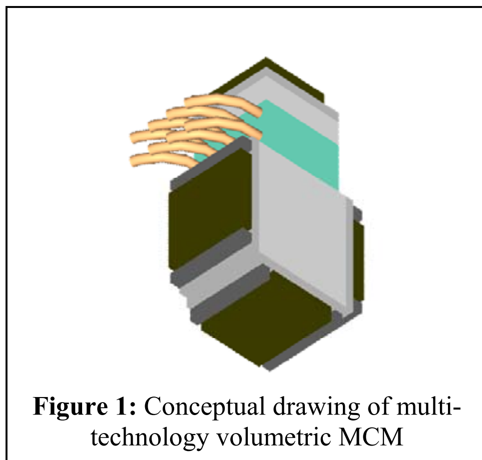

Figure 1: Conceptual drawing of multi-technology volumetric MCM

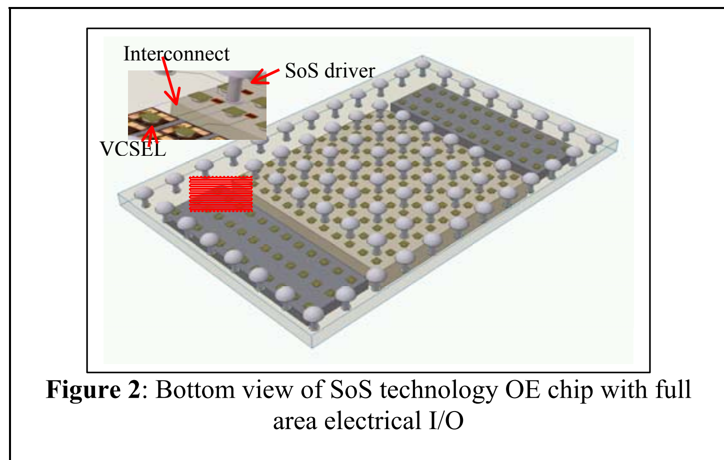

Figure 2: Bottom view of SoS technology OE chip with full area electrical I/O

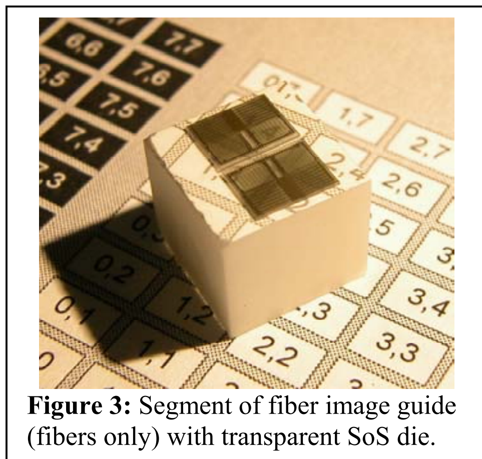

Figure 3: Segment of fiber image guide (fibers only) with transparent SoS die.

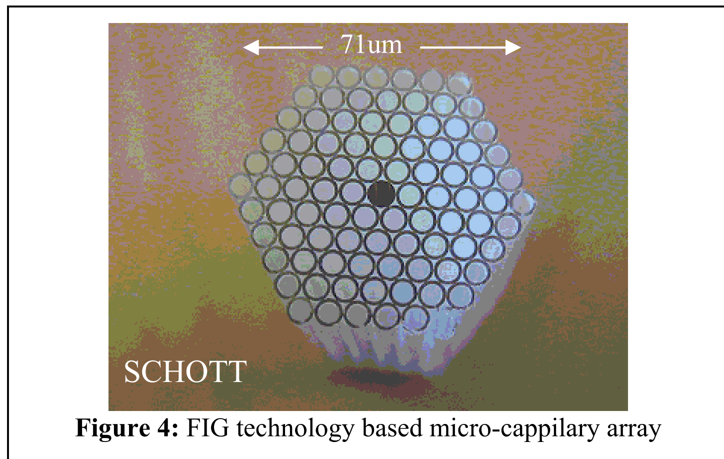

Figure 4: FIG technology based micro-cappilary array

References

1. Chiarulli, et. al., Applied Optics, Vol. 39, Issue 5 Page 698 (February 2000).
2. Chiarulli, et al. Optics in Computing, OSA Technical Digest 1999 , pp. 112-114.
3. Chiarulli, et al.. LEOS 2000. 13th Annual Meeting. IEEE , Volume: 2 , 2000 pp 423
4. Chiarulli et. al., Optics in Computing 2000, SPIE Vol. 4089, pp (2000) 80-85