ACTIVE SUBSTRATES FOR OPTOELECTRONIC INTERCONNECT

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ABSTRACT

We present the design of an intelligent optoelectronic chip carrier (IOCC). This is an active package that is the basis for short haul, PCB[1] and MCM[2,3] level, optical interconnect. Our goal is a new solution to one of the most difficult problems associated with the packaging of chip-level optical interconnections; the dense and spatially interleaved integration of optical signaling with electrical signals, power and ground. Our approach is based on an "active substrate" using Peregrine UTSi silicon on sapphire technology and the adaptation of laser drilling techniques to create vias through the sapphire. The result is an optoelectronic package that supports full CMOS performance, is mechanically and electrically compatible with current ball grid array (BGA) technology for electronic interconnect, and provides windows for active side optical I/O and substrate-side thermal extraction paths.

OVERVIEW

The I/O pad set for most contemporary VLSI components is a large array of area pads in which electrical I/O pins are distributed among a larger number, often as many as three or four times as many, power and ground pins. This spatial distribution of power and ground pins over the chip area and the close proximity between I/O and supply pins cannot be changed without impacting the I/O performance of the CMOS circuit. Any technique for augmenting these interconnects with an optical interconnection architecture must provide both a device interface and a connection structure that does not disturb this relationship.

Most of the optoelectronic VLSI packages and interconnection architectures proposed to date take one of two approaches. In one approach [fouad] the optical and electrical connections are segregated, with signal pins connected to optoelectronic devices by flip-chipping to the center of the device and power and ground connections drawn from the edges of the chip. In the other approach [], the optoelectronic and electronic device are mounted separately on a common substrate such as PCB or MCM material. The former is simply unrealistic since restricting power and ground connections to the edges of the chip severely limit device performance. In the latter, the electrical PCB/MCM substrate is a performance-limiting bottleneck.

In this paper we present and alternative design, an intelligent optoelectonic chip carrier (IOCC). The IOCC is mechanically compatible with existing ball grid array (BGA) technology and can be directly mounted onto an optoelectrontic PCB or similar MCM substrate. The only mechanical difference in the IOCC is that optical windows are embedded in the solder bump array for arrays of incoming and outgoing optical channels. Electrically the IOCC is quite different from a conventional BGA chip carrier. It is an active device, not a passive interconnect. It is fabricated on a Peregrine UTSi, Silicon on Sapphire (SoS), substrateand thus can include driver and receiver circuits as well as serialization, channel coding, and multiplexing logic in the package. By locating optical drivers directly below the contact pins for the CMOS devices, we can achieve the tightest integration and best performance possible with current technology.

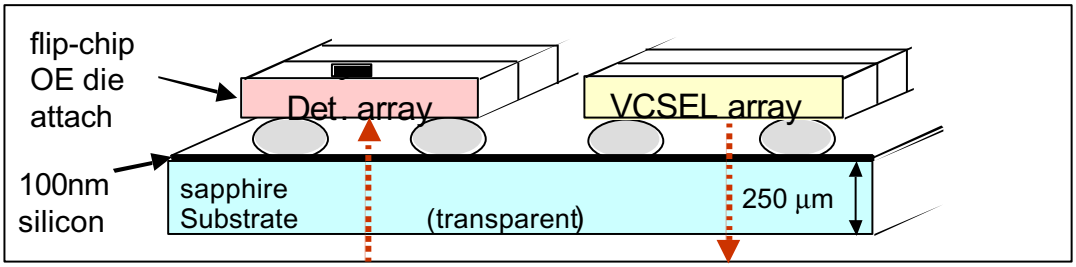

Figure 1: Example of UTSi O/E device structure. Optical signals enter and exit through the transparent substrate to flip-chip bonded OE devices

ACTIVE SUBSTRATE TECHNOLOGY

The active substrate of the IOCC is a Silicon-on-Sapphire (SoS) mixed signal device fabricated using the Peregrine UTSi process. VCSEL and detector arrays for optoelectronic interfaces are flip chip bonded to the top surface as shown in Figure 1 with emitters and detectors pointed down,

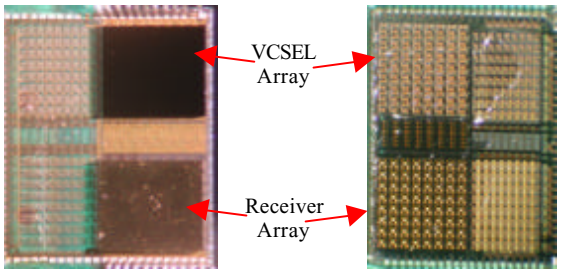

Figure 2: Photographs of 64 channel switch O/E switch designed at the University of Pittsburgh and fabricated by Peregrine The left image shows the top side, the right image shows the bottom side (flipped).

into the substrate. Since the sapphire is transparent, the optical channels traverse this material and enter or exit the chip from the bottom surface. This orientation has the key advantage over other optoelectronic architectures that the top it retains a thermal extraction path through the top of the device. SoS technology can host both digital and analog circuitry in the substrate. Unlike conventional silicon CMOS, the insulating sapphire material eliminates both substrate crosstalk and parasitic capacitance to the substrate. This enables the dense integration of multiple channels of analog drivers with receivers (TIAs and limiting amplifiers) and other sensitive analog circuitry with high speed digital circuitry serialization, encoding/decoding, ECC, and switching.

Figure 2 shows top and bottom view photographs of a 64 channel fiber optic switch using a 2D, 8x8, VCSEL array. The top view shows the transparent UTSi device and bonded OE arrays. On the left side of the chip is the CMOS circuitry for routing

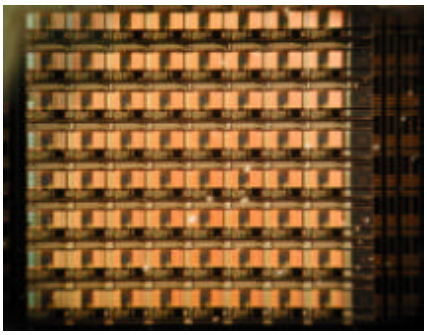

Figure 3: Bottom view looking through transparent substrate. Flip-chip bonded photodectors can be seen through windows opened in the SoS circuitry

signals from the receiver array (top right) to the transmitter array (bottom right). The bottom view shows windows left in the SoS circuitry for optical signals. Figure 3 is a close-up of the chip, where

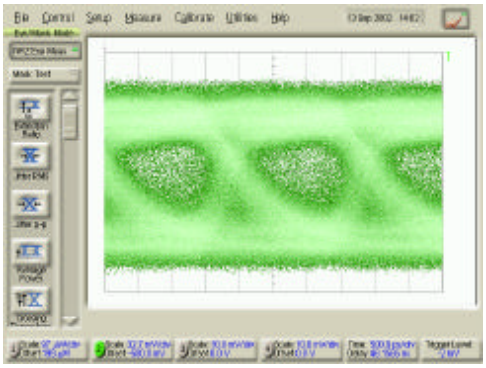

Figure 4: 500Mhz eye diagram for probed operation of the circuit in Figure 9. This shows receiver output for an optical signal that was coupled out of a FIG

the array of PIN detectors is clearly visible through the substrate windows. Receiver operation at 500Mhz is shown in the eye-diagram in Figure 12.

CHIP CARRIER DESIGN

Although the SoS substrate supports digital CMOS circuitry, as in the system above, it is not possible to match the density and performance of bulk CMOS in this process. Thus the IOCC is designed to have one or more CMOS dies flip-bonded to the

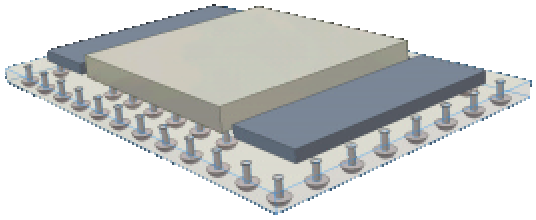

Figure 5: Top view of IOCC package

substrate along with the VCSEL and detector arrays. In order to support the electrical I/O requirements discussed above, as well as providing the stable, low noise power and ground supply

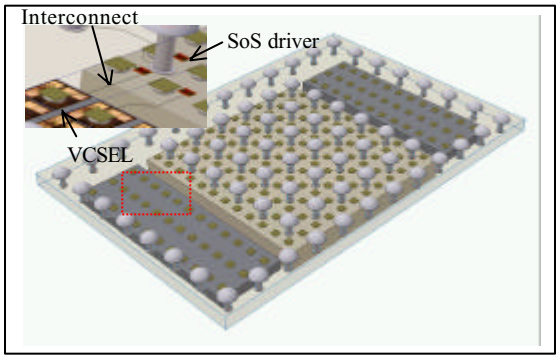

Figure 6: Bottom view of IOCC package

connections required for high-speed CMOS, the IOCC provides area pad connections on its bottom surface using laser-drilled vias through the sapphire substrate.

Figures 5 and 6 are conceptual drawings of the design. Figure 5 shows the top side with one CMOS die and two opto-electronic chips flip-chip bonded to the logic side of the SoS die. Figure 6 is a view from the bottom side. The transparent SoS substrate allows us to see in this view: the solder-ball array on the bottom side of the die, the vias that have been laser drilled and plated through the SoS substrate, and the bond pad arrays for the CMOS and optolelectronics interleaved with the via contacts on the logic side. The inset shows a close-up view that illustrates a CMOS bond pad with driver logic and interconnect routing to the VSCEL in the SoS. This arrangement, drawn to scale with a 500um pitch for the solder-ball/via array pitch and and 250um pitch for the flip-chip bond pads, leaves ample room on the logic side of the substrate for driver and receiver logic and interconnect through the metal layers of the SoS device.

There are two key features of the resulting structure. The first is that the substrate itself supports active devices, not passive routing. Thus, on the SoS substrate we can not only provide driver and receiver circuitry for the optoelectronic pathways, we can also provide buffering, bus control, level shifting, and driving among all of the chips on the substrate.

The second key feature of the IOCC is the implementation of electrical vias through the sapphire substrate to connect electrical signal, power and ground connections to solder balls on the bottom surface of the substrate. Sapphire is an extremely hard material and mechanical drilling techniques cannot be used. Our approach uses focused laser drilling to create vias using a 355nm laser housed in an ESI model 5300 laser drilling machine. This machine is capable of 2-4um positioning accuracy with can provide the necessary hole diameters of 60-80um in approximately five seconds of drilling time per hole. This process is the first application of large scale vias for packaging applications and the first use of post processing steps for SoS designed to provide plated metal contacts through these holes.

In our first demonstration device, we are designing an IOCC which will support a CMOS microcontroller die along with VCSEL and receiver arrays. The active substrate will provide level conversion, driving, receiving as well as multiplexing of signals between the microcontroller and the optoelectronics. The design will provide 36 to 48 optical channels that will be allocated to the major I/O bus of the microcontroller. The package itself will be mounted on a transparent substrate to allow it to

optically communicate with a second IOCC which will provide memory and system I/O.

SUMMARY

The need for ever increasing I/O bandwidth for VLSI systems drives us to consider optical I/O. However, to date most attempts to integrate optics with state-of-the-art VLSI integration levels incur severe penalties in the electrical I/O performance. Either both optical and electronic I/O must be segregated on the chip, to support flip-chip integration; or else multi-chip carriers must be used, degrading high speed signal integrity. Our solution is an optically transparent, electrically active substrate that enables tight integration of multiple chips, both standard CMOS devices with area pads, as well as optoelectonic devices. Electrical interconnects among devices are mediated by active devices, while optical interconnect between devices is through the transparent substrate. All I/O is preformed on the same common face of the substrate, allowing access to the backside of the devices for thermal management.

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