Monitoring and Synchronization of Chip2Chip Links

Luis Cordova, Cao Zhang, Duncan Buell

USCarolina
Cray XD1 Direct Connected Processor Architecture
Application Acceleration with FPGA-Based
Xilinx Virtex II Pro FPGA

- Virtex-II Pro FPGAs incorporates embedded PowerPC™ processors and 3.125 Gbps RocketIO serial transceivers. Introduced in 2003, Virtex-II Pro X FPGAs extended the transceiver data rate to 10Gbps.
Figure 1-1: RocketIO Transceiver Block Diagram
Design Diagram

- MicroBlaze 32-bit uP @ ~199 MHz
- MGT Controller (Peripheral 2)
- MGT (local link interface)
- RapidArray Controller (Peripheral 1)
- RT Core
- ~3.2 GB/s RapidArray Transport
- AMD Opteron
- Hobbit
- FPGA

Design Code

- Orange

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