Meeting times:  Officially MWF 12:20-1:10, but may change to MW 12:20-1:35

Locations:  Swearingen 2A15 (lecture), 1D43 (lab)

Textbook:  *CMOS VLSI Design: A Circuits and Systems Perspective*  
(3rd edition)  
Neil H.E. Weste, David Harris (ISBN: 0321149017)

Official prereqs:  Digital logic design (CSCE 211),  
Circuit analysis (ELCT 221)

Instructor:  Dr. Jason D. Bakos
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Office:  Swearingen 3A52
Webpage:  http://www.cse.sc.edu/~jbakos
Phone:  777-8627 (x7-8627)
Office hours:  Monday, Wednesday 11:00 – before class  
(However, stop in anytime I’m here!)

Grading structure:  Homework, lab assignments 50%  
Course Project 50%

Course Organization:

**Introduction:**  IC design, CMOS logic, and fabrication fundamentals  
2 weeks:  
Lectures  
Assignments from textbook

**CMOS circuit design, layout, and simulation**  
1 week:  
Tutorial:  Cadence IC-Tools  
2 weeks:  
Design projects

**Cell library development**  
2 weeks:  
Development of standard cell library  
2 weeks:  
Tutorials:  Cadence SignalStorm and Abstract Generator  
Report on cell library

**VHDL Design**  
1.5 weeks:  
Lectures on VHDL  
Tutorial:  Mentor HDL Designer

**Logic Synthesis and Place-and-Route**  
1.5 weeks:  
Tutorial:  Synopsys Design Analyzer  
Tutorial:  Cadence First Encounter

**Course project (Two member teams)**  
Remainder of term
**Official Policy on Late Submissions**

Late homework and lab assignments will be charged a 5% grade penalty for each weekday after the due date. Students that do not complete the final project by the end of the semester will not receive a passing grade except under special circumstances and with permission from the instructor.

**Academic Honesty Policy**

Students are encouraged to assist their colleagues for the purpose of overcoming technical challenges related to the use of the design tools. Moreover, students working on a group project must (by definition) perform joint work. However, any collaboration beyond these exceptions is prohibited and is subject to the university's guidelines, regulations, and policies regarding academic dishonesty.

**Students Receiving Graduate Credit**

University policy requires that students who wish to receive graduate credit for an undergraduate course must complete additional requirements beyond those who only wish to receive undergraduate credit. In order to receive graduate credit for this course, there will be additional required components and requirements for the final project design.

**Group Work Policy**

The final project will require students to work in groups of two. Choose your group partner wisely. Both partners will receive the same grade for the final project. The instructor is not responsible for inner-group conflicts related to disproportional work effort.