CSCE 613: FUNDAMENTALS OF VLSI CHIP DESIGN

End of Course Analysis and Outcomes

Fall 2006 – Jason D. Bakos

Catalog Description:

613 - Fundamentals of VLSI Chip Design. (3) (Prereq: ELEC 371) Design of VLSI circuits, including standard processes, circuit design, layout, and CAD tools. Lecture and guided design projects.

Textbook(s) and Other Required Material:

Neil H.E. Weste, David Harris, *CMOS VLSI Design: A Circuits and Systems Perspective* 3rd Ed., Addison Wesley 2006, ISBN: 0321149017.

Reference: http://www.cse.sc.edu/~jbakos/613 (tutorials and additional instruction for lab work)

Course Outcomes:

After completing this course students should be able to:

1. Design CMOS logic using MOSFET devices, perform circuit-level simulation of CMOS logic gates to determine logic delay
2. Characterize MOSFET devices for I-V behavior, gate and parasitic capacitance, and effective resistance
3. Design a library of standard logic, driver, and memory cells using schematic capture, layout, DRC, extraction, layout-vs-schematic, library characterization, and abstract generation
4. Design large-scale digital logic systems using VHDL behavioral design and simulation: 16-bit arithmetic logic unit that performs bit-wise logic, shifting, rotation, fast addition, fast subtraction, multiplication, and division
5. Synthesize, place-and-route, and generate cell and interconnect delay models for VHDL designs using their custom-designed standard cell library

Topics Covered:

- CAD/EDA design flow (spanning circuit-level, logic-level, and system-level)
- Design methodologies and techniques
- Logic delay and delay models
- CMOS logic design
- MOSFET semiconductor theory
- Circuit simulation
- Logic verification
- Standard cell library design
- Managing design complexity of large-scale digital systems
- Behavioral design of arithmetic logic unit (bit-wise logic, shifting, rotating, fast addition, fast subtraction, multiplication, division)

Assessment of Learning by Course-Outcome:

Summary of Results

Coursework	Topic	Outcomes																			
		OC. 1				OC. 2				OC. 3				OC 4				OC. 5			
		CE	CS	EE	Grad	CE	CS	EE	Grad	CE	CS	EE	Grad	CE	CS	CIS	Grad	CE	CS	EE	Grad
HW #1	CMOS logic design	.62			.92																
Lab 1	Characterize CMOS gate delays using circuit simulation					.73			.88												
Lab 2	Characterize I-V behavior of MOSFET devices					.75			.92												
Lab 3a/b	Characterize C_g for MOSFET devices, characterize C_d for MOSFET devices					.93			.98												
Lab 4	Standard cell library design and characterization									.89			.95								
Lab 5	HDL design, verification, synthesis, place-and-route, and delay characterization of 16-bit ALU													.68			.70	.68			.70
Average																					

* Averages based on 4 Computer Engineering, 0 Computer Science, 0 Electrical Engineering, 10 graduate students who completed the course.

Outcome 1. ***Design CMOS logic using MOSFET devices, perform circuit-level simulation of CMOS logic gates to determine logic delay.***

Coverage of Material

The first homework and first lab are designed to measure this outcome.

Measurements

Homework 1 consists of a sequence of exercises where the student must perform paper-and-pencil design of CMOS logic at both the transistor-level and gate-level.

Lab 1 requires the student to use simulation techniques to determine the logic delay of a CMOS inverter using two methods. In the first method, the student designs and simulates an FO4 (fanout-of-4) test circuit that produces a realistic input slope and includes realistic load conditions. The student uses this method to determine the delay when using two different supply voltages. For the second method, the student designs and simulates a 31-stage ring oscillator to determine its period (and thus the delay of each inverter in the ring). The student also performs this test using two different supply voltages.

Outcome 2. ***Characterize MOSFET devices for I-V behavior, gate and parasitic capacitance, and effective resistance***

Coverage of Material

The second and third labs are designed to measure this outcome.

Measurements

Lab 2 requires the student to design and simulate test circuits to characterize the I-V behavior of the NMOS and PMOS devices. To do this, the student uses the circuit simulator to perform a DC-sweep analysis to measure I_d current for five fixed V_{gs} values over a sweep of V_{ds}. The student then performs a DC-sweep analysis to measure I_d for a fixed V_{ds} over a sweep of V_{gs}.

Lab 3a requires the student to use simulation techniques to determine C_g (per micron of width) and effective resistance for MOSFET devices. The student determines C_g by matching the delay between an inverter driving a load inverter versus an inverter driving a load capacitor. Next, the student must derive the relationship between the total C_g of a MOSFET and the corresponding effective resistance over the switching period. The student performs this by measuring the difference in delay between an FO4 and FO3 inverter. Using the RC delay model, the student uses this delay difference to determine the relationship between C_g and effective resistance.

Lab 3b requires the student to use simulation techniques to determine C_d (per micron of width) for the MOSFET devices. This student determines C_d by matching the delay between an inverter driving a drain of a MOSFET device in the cutoff region versus an inverter driving a load capacitor.

Outcome 3. ***Design a library of standard logic, driver, and memory cells using schematic capture, layout, DRC, extraction, layout-vs-schematic, library characterization, and abstract generation***

Coverage of Material

The forth lab is designed to measure this outcome.

Measurements

Lab 4 requires the student to fully design, characterize, and package a standard cell library that he or she will use later in the course as a target to synthesize HDL descriptions of large-scale digital systems.

The lab requires the student to design, simulate, and verify each logic, memory, driver, and transmission gate cell in both schematic and layout form. This includes the use of schematic capture, layout design, design rule checking, layout extraction, layout-vs-schematic checking, and circuit simulation of schematics and extracted layouts. Next, the student must characterize their library with a characterization tool. Finally, the student must generate abstract (black box) views for each cell layout for use with the place-and-route tool. This step requires that the student design their cell layouts to be ready for design automation (i.e. designed to snap-together and conform to a place-and-route grid for geometries and pin locations).

Outcome 4. ***Design large-scale digital logic systems using VHDL behavioral design and simulation: 16-bit arithmetic logic unit that performs bit-wise logic, shifting, rotation, fast addition, fast subtraction, multiplication, and division***

Coverage of Material

The first part of the fifth lab is designed to measure this outcome.

Measurements

The first part of Lab 5 requires the student to design a 16-bit ALU microarchitecture using a hardware description language. The student must also design a corresponding simulation test bench to verify the functionality of his or her design. The purpose of these requirements is for the students to learn large-scale digital design and verification methodology (along with basic computer arithmetic and control design).

Outcome 5. ***Synthesize, place-and-route, and generate cell and interconnect delay models for VHDL designs using their custom-designed standard cell library.***

Coverage of Material

The first part of the fifth lab is designed to measure this outcome.

Measurements

The second part of Lab 5 requires the student to fully implement their ALU design using logic synthesis and place-and-route. This part of the lab gives the student experience in using industrial electronic design automation tools to implement a large-scale digital system. The students must provide the synthesis tool with performance constraints and use the tool to generate cell and interconnect delay models. The result of this is a design formed from placed and interconnected cells from the students' own custom-designed cell library.

Grade Distribution from Fall 2006:

Grade	CE	Grad
A	2	5
B+		
B	1	4
C+		
C		
D+		
D		
I	1	1
F		

Changes

December 2006:
When I took over teaching this course, I performed an extensive redesign and update of the course. I am not familiar with the previous incarnation of the course.
-Jason D. Bakos

Major Changes

N/a.

Minor Changes

N/a.

Planned Changes

None.

Effect on Outcomes

N/a.