Meeting times: Tuesday, Thursday 12:30 – 1:45
Locations: Swearingen 2A19 (lecture), 1D43 (lab)

Textbook: *CMOS VLSI Design: A Circuits and Systems Perspective* (3rd edition)
Neil H.E. Weste, David Harris (ISBN: 0321149017)

Official prereqs: Digital logic design (CSCE 211),
Object-oriented programming (CSCE 245)

Preferred prereqs: Circuit theory

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Office hours: Tuesday, Thursday 11:00 – 12:30
(However, stop in anytime I’m here!)

Grading structure:
Assignments/labs  40%
Course Project   60%

Course organization:

**Introduction: IC design, CMOS logic, and fabrication fundamentals**
2 weeks:
Lectures
Assignments from textbook

**CMOS circuit design, layout, and simulation**
1 week:
Tutorial: Cadence IC-Tools
2 weeks:
Design projects
2 weeks:
Development of standard cell library

**Cell library development**
2 weeks:
Tutorials: Cadence SignalStorm and Abstract Generator
Report on cell library

**VHDL Design**
1.5 weeks:
Lectures on VHDL
Tutorial: Mentor HDL Designer
2 weeks:
Design project

**Logic Synthesis and Place-and-Route**
1.5 weeks:
Tutorial: Synopsys Design Analyzer
Tutorial: Cadence First Encounter

**Course project**
Remainder of term