CSCE 611: Advanced Digital Design:
Fall 2024
Updated 8/26/24

1 Catalog Description

Design techniques for logic systems; emphasis on higher-level CAD tools such as hardware description languages and functional modeling. Prerequisites: CSCE 212

2 Meeting Times

Section	Lecture	Lab
Section 001	M 3:55-5:10 in Swearingen 2A14	W 3:55 to 5:10 in Swearingen 3D22
Section 002	M 3:55-5:10 in Swearingen 2A14	F 3:55 to 5:10 in Swearingen 3D22

3D22 combination: 4-5-2-1-3

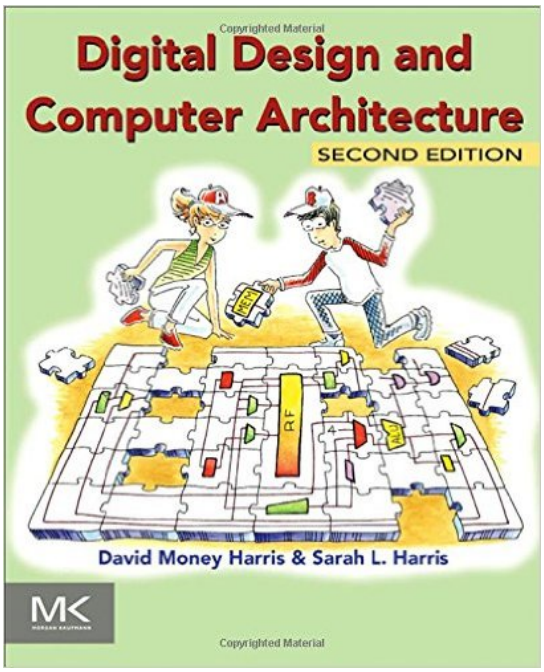
3 Electronic Resources

1. Project submission, grade dissemination, up-to-date schedule, downloads, announcements, links to useful information, project descriptions are disseminated via the CSE Moodle "Dropbox" site, http://dropbox.cse.sc.edu (not Blackboard).
2. Lecture recordings: https://youtube.com/c/JasonBakos
3. We will use electronic design software installed in the CSE departmental computer labs. The CSE labs are currently located in Swearingen 1D43 and 3D22. Be sure you can log into the lab computers in 3D22.
4. Urgent course announcements are broadcast on the website and to your university e-mail (@email.sc.edu). Please regularly check (or forward) this e-mail address.
5. Each team must find their own preferred method for collaborating (e.g. GitHub, Dropbox, etc.).

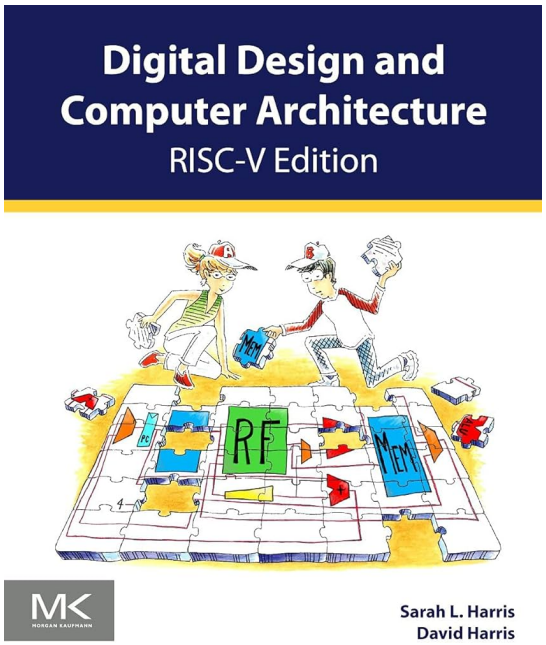
Contact Ryan Austin (rmaustin@cse.sc.edu) for Moodle and lab support.

4 Textbook

Digital Design and Computer Architecture 2/e
by David Harris and Sarah Harris
Morgan Kaufmann (Elsevier) Publishers
(Required text, but a PDF is available online.)



(a) MIPS Version



(b) RISC-V Version

Figure 1: Textbook covers

5 Course Learning Outcomes

- Perform HDL design: Design large-scale digital systems using Verilog
- Perform simulation and verification: Perform behavioral verification using test benches and simulation
- Design microarchitectures: Design a pipelined microprocessor that implements the MIPS instruction set
- Design interconnects: Design a system bus architecture with CPU, memory, and I/O interfaces
- Perform logic synthesis: Synthesize, place-and-route, and implement a computer system on a programmable hardware platform

6 Important Dates

Date	**Day of Week**	**Notes**
Aug. 21,23	Wednesday, Friday	Lab canceled (semester spin up)
Aug. 26	Monday	Last day to change/drop a course without a grade of "W" being recorded
Sept. 2	Monday	Lecture canceled (Labor Day)
Oct. 14-18	Monday, Wednesday, Friday	Lecture and labs canceled; fall break
Oct. 21-25	Monday to Friday	Online midterm exam
Nov. 6	Wednesday	Last day to withdraw
Nov. 25, 27, 29	Monday, Wednesday, Friday	Lecture and labs canceled; Thanksgiving break
Dec. 4	Monday	Last lecture
Dec. 6	Wednesday, Friday	Last lab
Dec. 6	Friday	Project submission cutoff
Dec. 9-13	Monday to Friday	Online final exam

7 Instructors and Teaching Assistants

Instructor:	Jason D. Bakos
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Office hours:	by appointment

8 Grading Structure

Task	**Undergraduate**	**Graduate**
Lab 1: RISCV Program	12.5%	12.5%
Lab 2: 7-Segment Decoder	17.5%	12.5%
Lab 3: RISCV CPU with R/I/U-type instructions	17.5%	12.5%
Lab 4: RISCV CPU with SB/UJ-type instructions	17.5%	12.5%
Graduate/Honors Project: VLIW	n/a	15%
Quizzes	17.5%	17.5%
Midterm	17.5%	17.5%
Final exam	17.5%	17.5%
Total	**117.5%**	**117.5%**

Grade weights add up to 117.5% to allow for opting out of (for example) the last lab or the final exam.

9 Approximate Schedule

Week	**Lecture**	**Lab**
8/28	Introduction and RISCV ISA	Lab 1: RISC-V programming
9/4	None (Labor Day)	
9/11	RISCV ISA and SystemVerilog	
9/18	SystemVerilog and Simulation	Lab 2: 7-Segment Decoder
9/25	SystemVerilog Processes (always statement)	
10/2	Sequential Logic and RAM	
10/9	RISCV Datapath: Arithmetic	None
10/16	RISCV Datapath: Branch/Jump	Lab 3: RISCV CPU with R/I/U-type Instructions
10/23	RISCV Datapath: Branch/Jump	
10/30	Midterm	
11/6	Sequential Logic	Lab 4: RISCV CPU with SB/UJ-type Instructions
11/13	Digital Building Blocks	
11/20	Digital Building Blocks	None (Thanksgiving)
11/27	Timing Analysis	
12/4	CMOS Logic	

10 Disability Support

The University of South Carolina is committed to providing access to programs and services for qualified students with disabilities. If you are a student with a disability and require accommodation to participate and complete requirements for this class, notify me immediately and contact the Student Disability Resource Center (http://www.sa.sc.edu/sds, 1705 College Street, Close-Hipp, Suite 102, 803-777-6142, sasds@mailbox.sc.edu) for verification of eligibility and determination of specific accommodations. In addition, please provide me the required accommodation letter from the Student Disability Resource Center. All course materials are available in alternative format upon request.

11 Syllabus Change Policy

This syllabus is a guideline for the course and is subject to change with reasonable notice.

12 Grading scale

Grade	Criteria
A	$90 \leq score \leq 115\%$
B+	$85 \leq score < 90\%$
B	$80 \leq score < 85\%$
C+	$75 \leq score < 80\%$
C	$70 \leq score < 75\%$
D+	$65 \leq score < 70\%$
D	$60 \leq score < 65\%$
F	$score < 60\%$

13 Academic Honesty Policy

Students are encouraged to assist their colleagues for the purpose of overcoming technical challenges related to the use of the design tools (foreshadow: like many industrial CAD/EDA tools, the tools we use are non-intuitive, generate meaningless error messages, are unstable, and are poorly documented).

Also, the members of each group are expected to work cooperatively and make nearly equal contributions toward each project.

Any collaboration beyond these exceptions is prohibited and is subject to the university's guidelines, regulations, and policies regarding academic dishonesty.

See the USC Honor Code at bit.ly/USCHonorCode.

Any student caught committing an Honor Code violation will receive a grade of 0 for the corresponding assignment or exam and the instructor will report the violation to the Office of Academic Integrity.

14 Lecture and Lab Attendance Policy

Attendance in lecture and labs is optional but highly encouraged. Lectures will usually appear on Youtube within 24 hours.

Note that the four projects will generally require more than the two lab periods (150 minutes) or three (225 minutes) periods allocated to each project. Significant lab work outside of scheduled lab time may be necessary to complete the projects on time. We suggest that students start each project outside of class time to get the most benefit from TA assistance during the latter part of their project work.

15 Group Work Policy

Group sizes of two are preferred, but group sizes of one are allowed based on enrollment and hardware availability. Three-member groups are not allowed.

Choose your group partner wisely. Both members of each group will receive the same grade for all projects.

16 Project Submissions

- Submitted projects must compile (both hardware and software) to receive partial credit.
- Only one member of each project group need submit each project. Project scores are assigned to each member of the group.
- Each project grade is assigned in part or in whole based on a project demonstration by the project group. All group members must be present for the project presentation.
- Students must submit each project on Dropbox by 11:59PM on the due date to receive full credit.
- Late projects are charged a 5% grade penalty for each school day after the due date, limited to a maximum of 30%. This way, projects submitted more than six days late are still subject to a 30% late penalty. This penalty is deducted from the raw score of the submission, so a one-day late submission earning a raw score of 80% will have a final score of 80% x 95% = 76%.

  Late penalties are based on the date and time at which the project is submitted (uploaded) to Moodle, NOT the date and time of the project demonstration. This way, students may demonstrate a project at any time after project submission without accruing late penalty. However, students must demonstrate the same version of the project that is submitted, and the project will not receive a grade until after the project is demonstrated.
- At most, each group may only submit one version of any project; no resubmissions are allowed.
- Any projects not submitted and demonstrated by 11:59pm on Saturday, Dec. 6 will receive a score of 0 without a documented medical excuse.