**Objective**
In this lab you will expand the EX and WB stages of your MIPS pipeline to add support for the following instructions:

- Arithmetic: *addi, addiu*
- Logical: *andi, ori, xori*
- Shift: *lui*
- Comparison: *slti*
- Load/store: *lw, sw*

**Testing Procedure**
Test your instructions using the test program from the slides.

Next, write a second test program that performs the following:
1. read an array of eight words (as unsigned integers) from your data memory (from addresses 0 through 7),
2. add the values to compute their sum,
3. divide the sum by 8 (rounding down) by shifting the sum three bits to the right,
4. display the result on the 7-segment displays, and
5. store the result to address 8.

You may assume that the sum of the eight words from memory will not overflow a 32-bit unsigned integer (0 to 4,294,967,295).

You may assume the average will not overflow the range of values allowable on the eight 7-segment displays (0 to 99,999,999).

Submit your projects through the course Moodle site (http://dropbox.cse.sc.edu). Upload all Verilog source and assembly files.