CSCE 313
Lab 4
Multiprocessor Image Transformation
Due Date: 3/30, 11:59pm

Design Requirements
The objective of this lab is to measure the performance impact of executing lab 3 on multiple processor cores.

Specific Tasks:
1. Add a second NIOS II/f processor, second JTAG UART, two mailboxes, and two corresponding on-chip memories to your SOPC Builder project
2. Set up your Avalon interconnect such that both processor cores are masters of all peripherals except for the JTAG UARTs, which are connected only to their respective CPUs
3. Each processor core will share the SDRAM but make sure the linker confines the code to two non-overlapping address ranges (see slides)
4. Make sure that both processors read the original image from flash
5. Change your Lab 3 code such that each processor will transform half the rows of the original image using barriers to keep the processors synchronized
6. Using the performance counter, calculate the speedup as compared to the single processor version of the code and report your results in an attached document. Use the fixed-point version of your code and adjust your cache size to ensure that both processors fit on the FPGA.

Project Submission
Each group must submit a report that lists the performance results.