Spring 2009 CSE Qualifying Exam

January 31, 2009
Architecture

1. Consider the following three hypothetical processors, which we characterize with a SPEC benchmark:

   (a) A simple MIPS two-issue static pipe running at a clock rate of 2 GHz and achieving a pipeline CPI of 0.6. This processor has a cache system that yields 0.0025 misses per instruction on average.

   (b) A deeply pipelined version of the two-issue MIPS processor with slightly smaller caches and a 2.5 GHz clock rate. The pipeline CPI of the processor is 0.8, and the smaller caches yield 0.0055 misses per instruction on average.

   (c) A speculative superscalar with a 64-entry window but achieves an average issue rate of 3.5. This processor has the smallest caches, which lead to 0.01 misses per instruction, but it hides 25% of the miss penalty on every miss by dynamic scheduling. This processor has a 1.5 GHz clock.

   Assume that the main memory time (which sets the miss penalty) is 50 ns. Determine the relative performance of the three processors. Hint: processor CPI can be computed by adding the pipeline CPI and cache CPI.

2. Three enhancements with the following speedups are proposed for a new architecture:

   - Speedup1 = 20
   - Speedup2 = 10
   - Speedup3 = 8

   Only one enhancement is usable at a time.

   (a) If enhancements 1 and 2 are each usable for 25% of the time, what fraction of the time must enhancement 3 be used to achieve an overall speedup of 10?

   (b) Assume the enhancements can be used 25%, 35%, and 10% of the time for enhancements 1, 2, and 3, respectively. For what fraction of the reduced execution time is no enhancement in use?

3. Suppose we have an application running on a 32-processor multiprocessor, which has a 800 ns time to handle reference to a remote memory. For this application, assume that all the references except those involving communication hit in the local memory hierarchy. Processors are stalled on a remote request, and the processor clock rate is 1 GHz. If the base IPC (assuming that all references hit in the cache) is 4, how much faster is the multiprocessor if there is no communication versus if 0.4% of the instructions involve a remote communications reference?
Algorithms

1. You are given an unsorted array of $n$ items with numeric keys, and you need to make $k$ searches of the array. (A search means finding the item with a given key value, if it exists.) You have two options:

   (a) Conduct $k$ many linear searches of the array.
   (b) Sort the array first using some optimal comparison-based sort, then conduct $k$ many binary searches of the array.

   Asymptotically in $n$, how big must $k$ be before the second option is more efficient? Give your answer using $\Theta(\cdots)$ notation, where “$\cdots$” is some function of $n$ that is as simple as possible. (You may reasonably assume worst-case behavior for all operations and that a single key probe (comparison) takes $O(1)$ time.)

2. Describe an algorithm that takes a directed acyclic graph $G = (V, E)$ and two vertices $s, t \in V$ and returns the number of distinct directed paths from $s$ to $t$. Your algorithm should run in time $O(|V| + |E|)$, although you need not prove this.

   You may assume that a $O(|V| + |E|)$-time topological sorting algorithm is available for you to use as a subroutine, which arranges the vertices of $V$ into a list $\langle v_1, \ldots, v_{|V|} \rangle$ such that if $(v_i, v_j) \in E$ then $i < j$. (You cannot assume anything more about the subroutine.)

3. Let 2-OF-5-SAT be the following decision problem:

   **Instance:** A Boolean formula $\varphi$ in conjunctive normal form where each clause has exactly five literals.
   **Question:** Is there a truth assignment to the variables of $\varphi$ such that each clause contains at least two true literals?

   2-OF-5-SAT is clearly in NP. Show that 2-OF-5-SAT is NP-complete by giving a polynomial reduction from 3-CNF-SAT (otherwise known as 3-SAT) to 2-OF-5-SAT. Briefly explain why your reduction works.