HIGH-RATE STATE ESTIMATION OF A PRINTED CIRCUIT BOARD UNDER SHOCK USING AN FPGA-DEPLOYED NEURAL NETWORK

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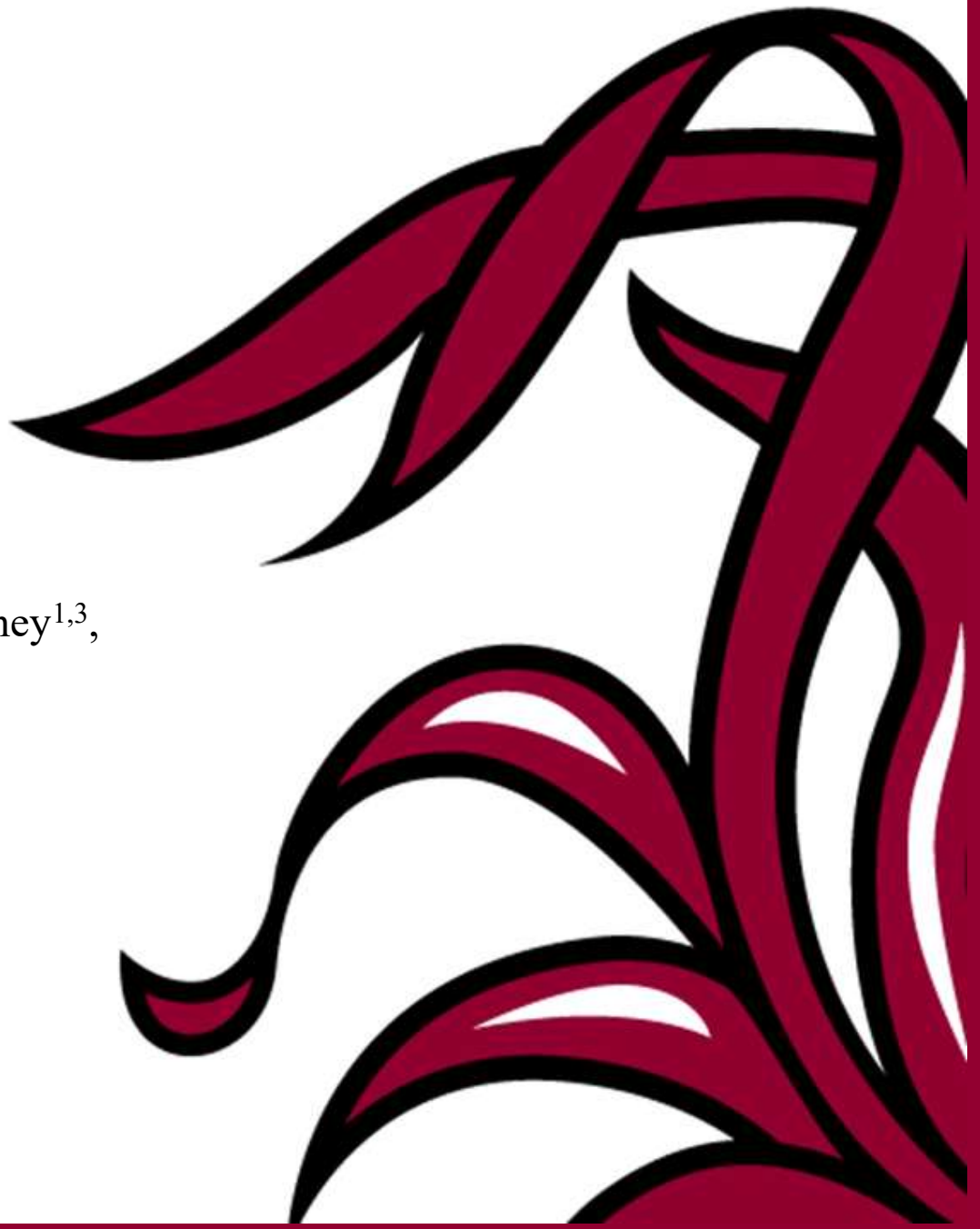
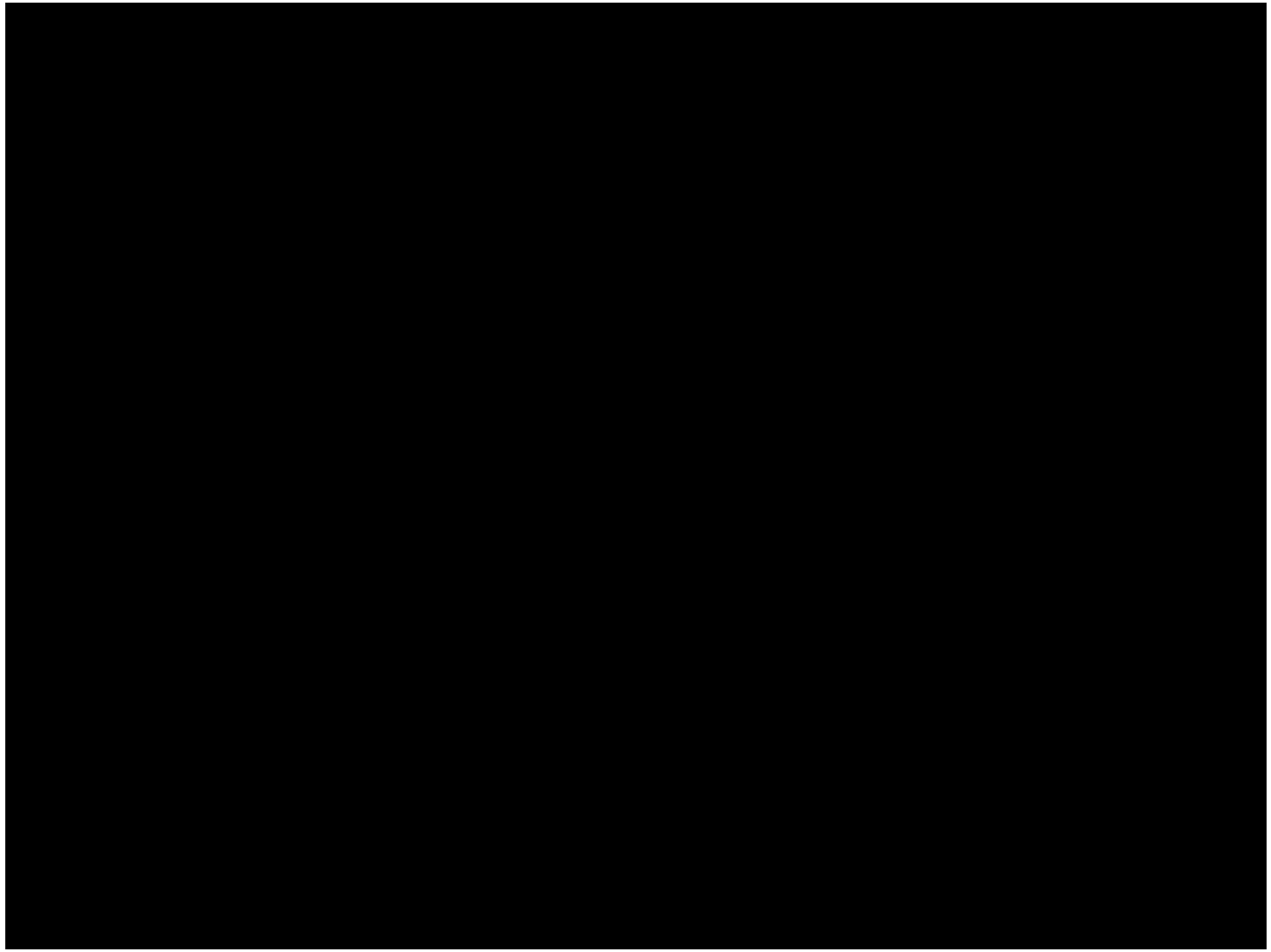


OVERVIEW

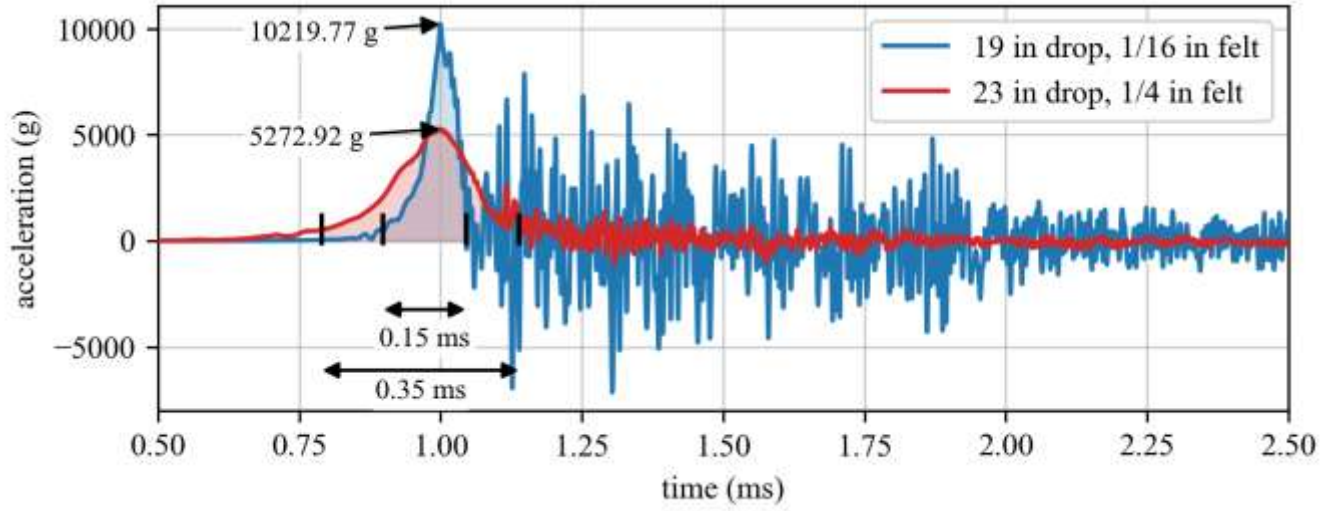
- Introduction
- Ongoing Work
- Focused Study
  - Objective
  - Experimental Dataset
  - Model Architecture
  - Model Training
  - FPGA Implementation
  - Performance
- Future Work

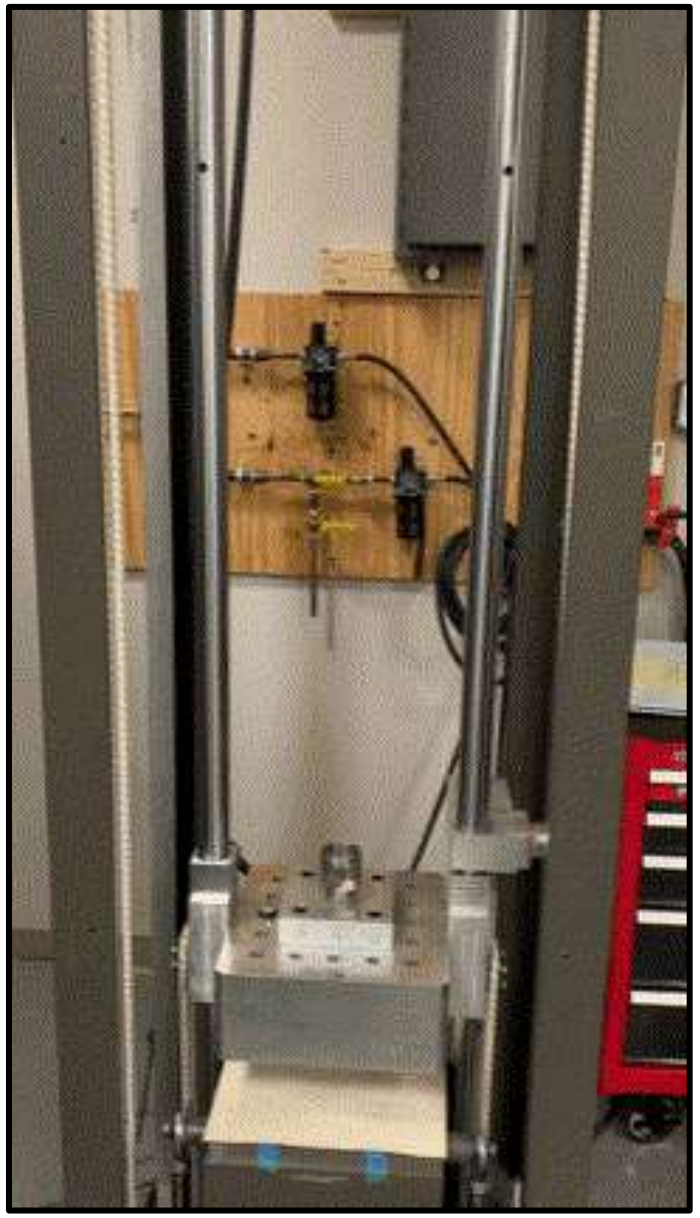


INTRODUCTION

HIGH-RATE SHOCK

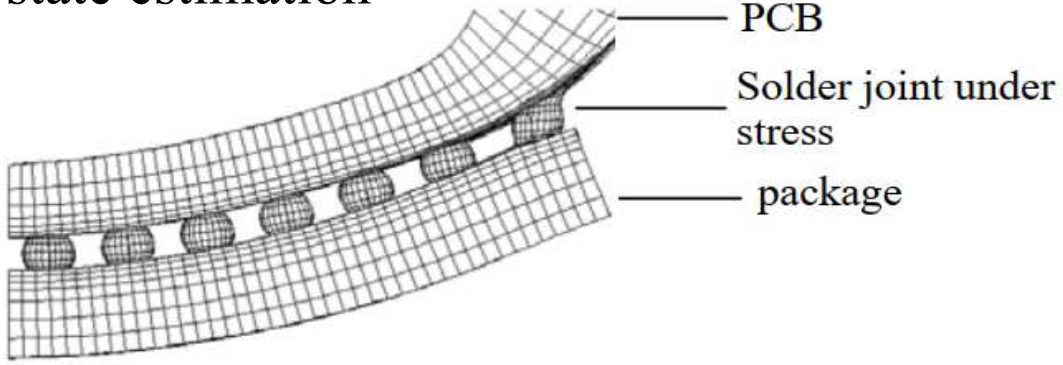
- Sudden, high-amplitude acceleration impulse (μs–ms duration)
- Broadband excitation with significant high-frequency content
- Generates extreme stress gradients and localized damage mechanisms
- Highly non-stationary and sensitive to boundary conditions
- Difficult to model and predict





ELECTRONIC ASSEMBLIES UNDER SHOCK

- PCBs are the structural and electrical backbone of nearly all modern electronic systems
- Board bending concentrates stress at package interconnects
- Solder joints, traces, and pads are susceptible to progressive damage
- High-rate response data can support earlier state estimation

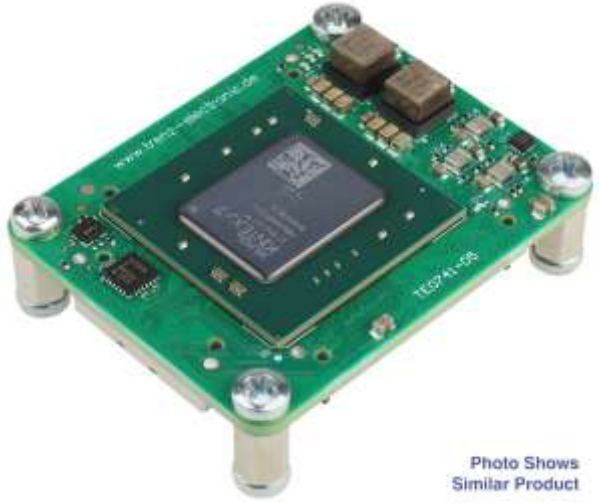


Seah, S. K. W., Wong, E. H., Ranjan, R., Lim, C. T., and Mai, Y. W., 2005, "Understanding and testing for drop impact failure," ASME Pacific Rim Technical Conference and Exhibition on Integration and Packaging of MEMS, NEMS, and Electronic Systems, pp. 1089-1094.

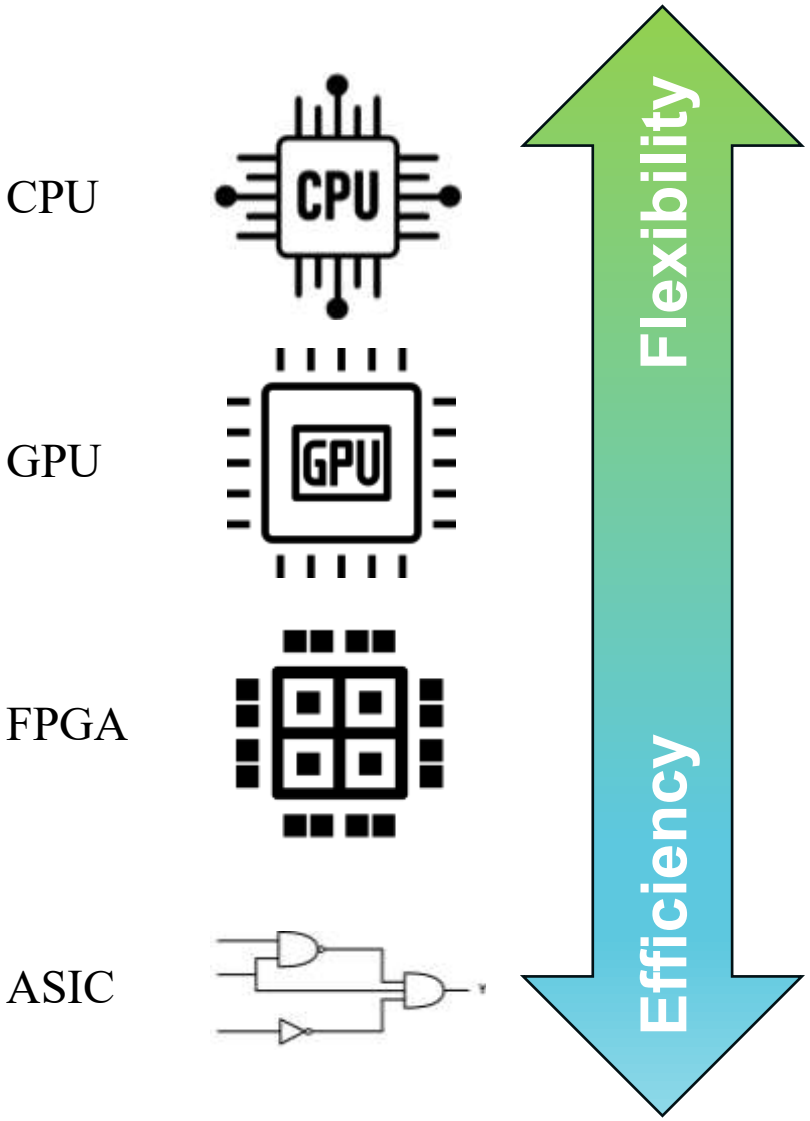
WHY AN FPGA?

Field programmable gate arrays (FPGA) map a fixed model into dedicated hardware for predictable embedded inference.

- CPU/GPU execution is flexible, but timing can vary
- ASICs are efficient, but fixed-function and costly to redesign
- FPGAs provide reconfigurable hardware with bounded latency
- On-chip memory keeps model parameters close to computation
- Hardware parallelism can be tailored to the model architecture



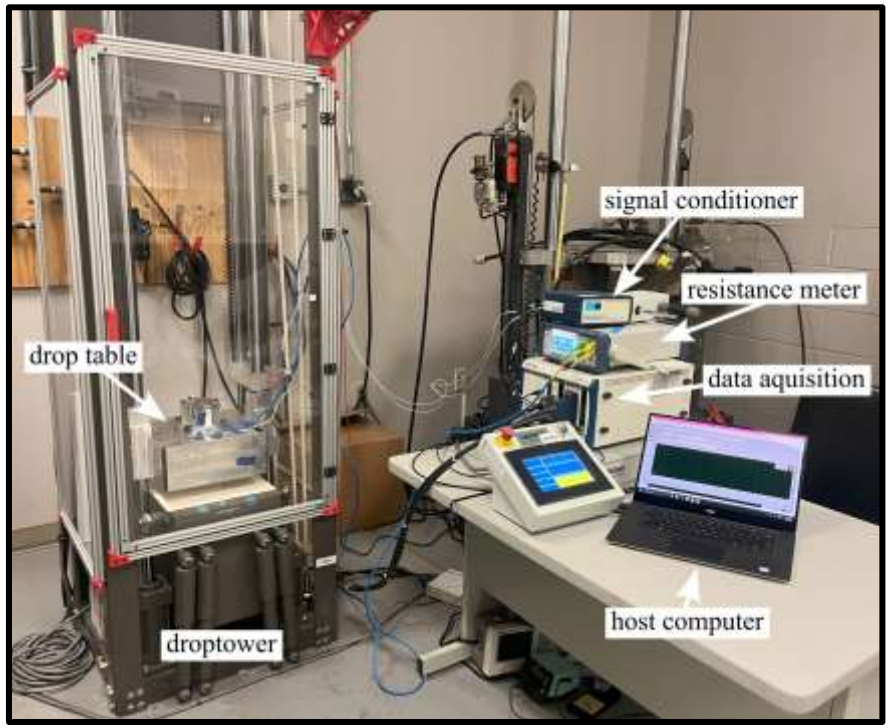
Kintex-7 K70T-2C

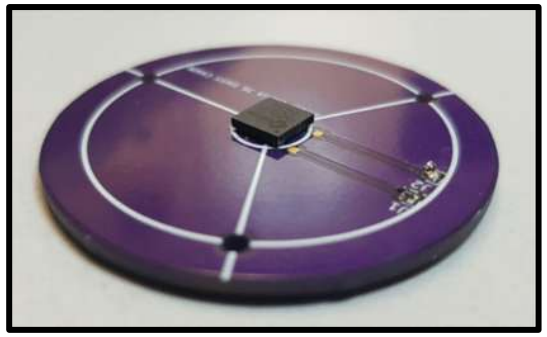


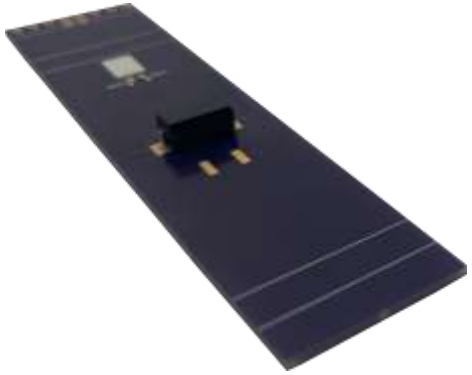
ONGOING WORK

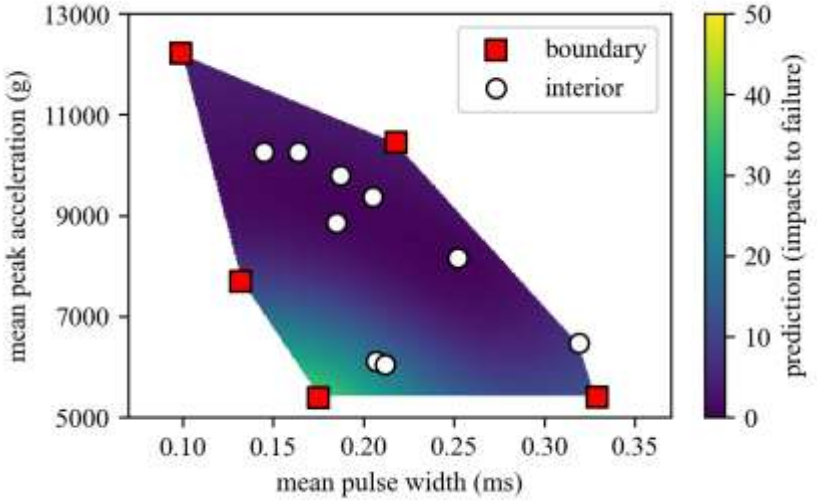
EXPERIMENTAL PLATFORMS

- Shock testing across multiple PCB geometries (circular, cantilever, fixed–fixed)
- Component-level fatigue studies (resistors, BGA dummy components)
- Controlled variation of impact energy and boundary conditions
- Creation of labeled, high-rate degradation datasets
- Kriging-based models guide adaptive test selection and predict failure boundaries

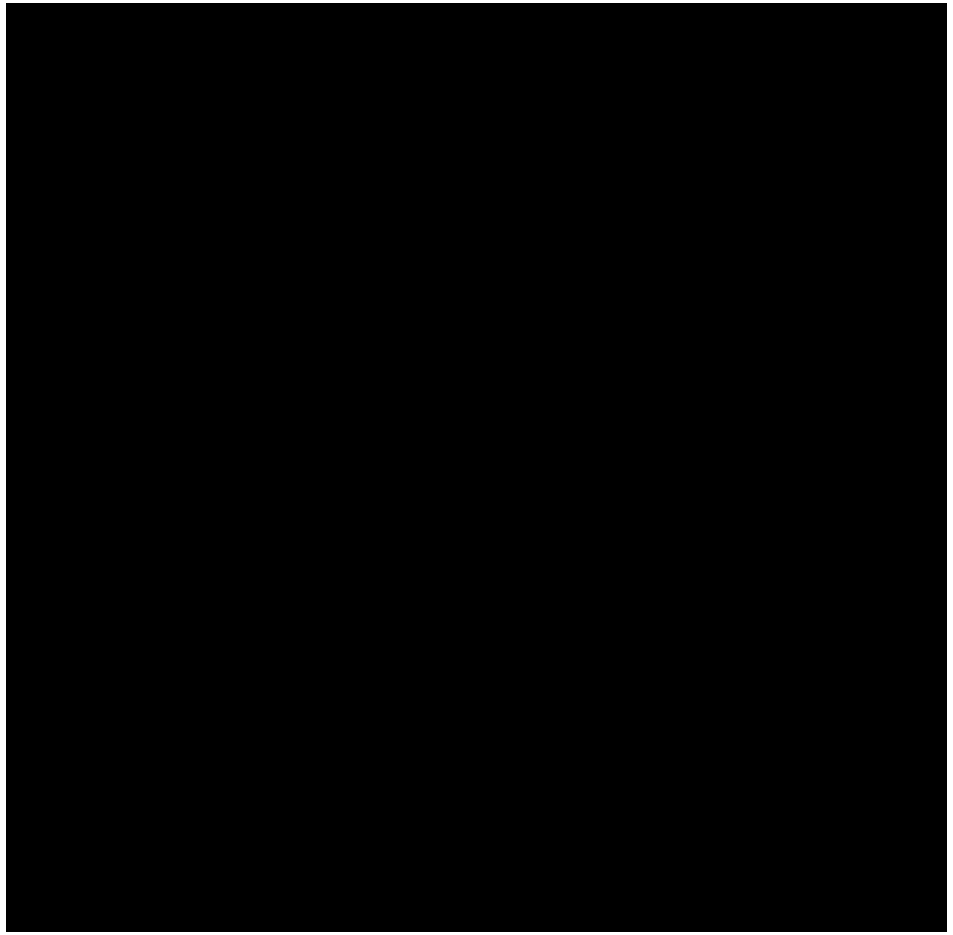


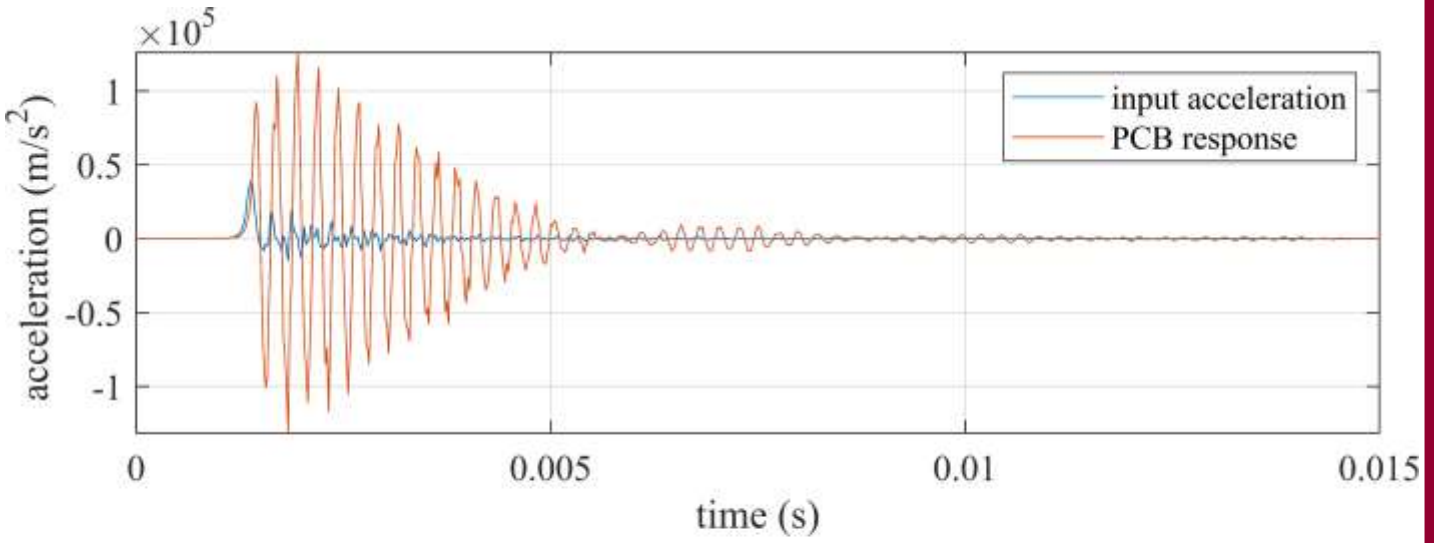


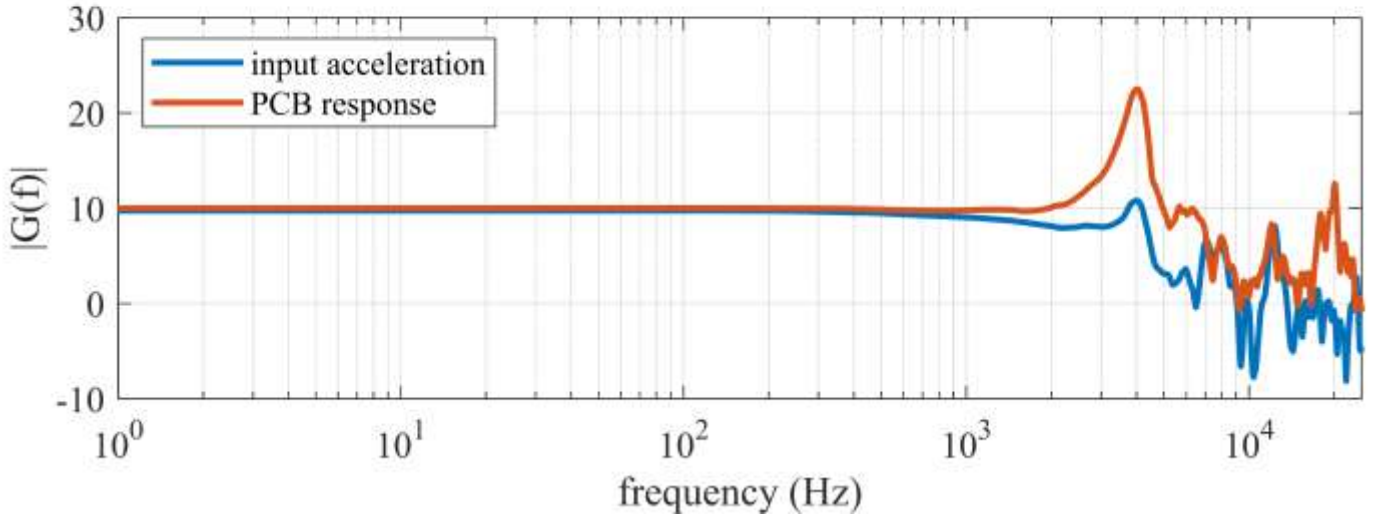




DATASET COLLECTION



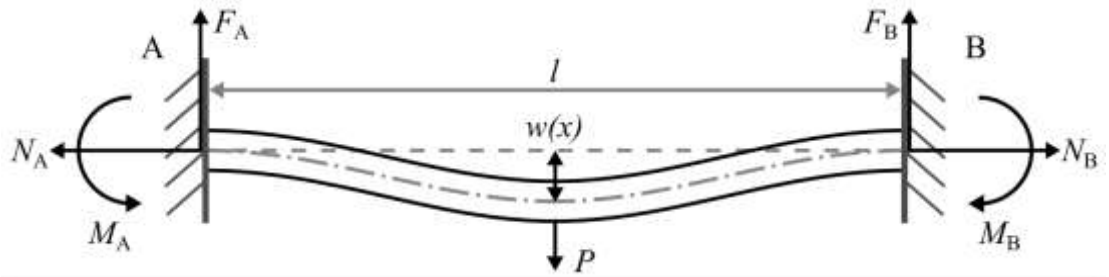


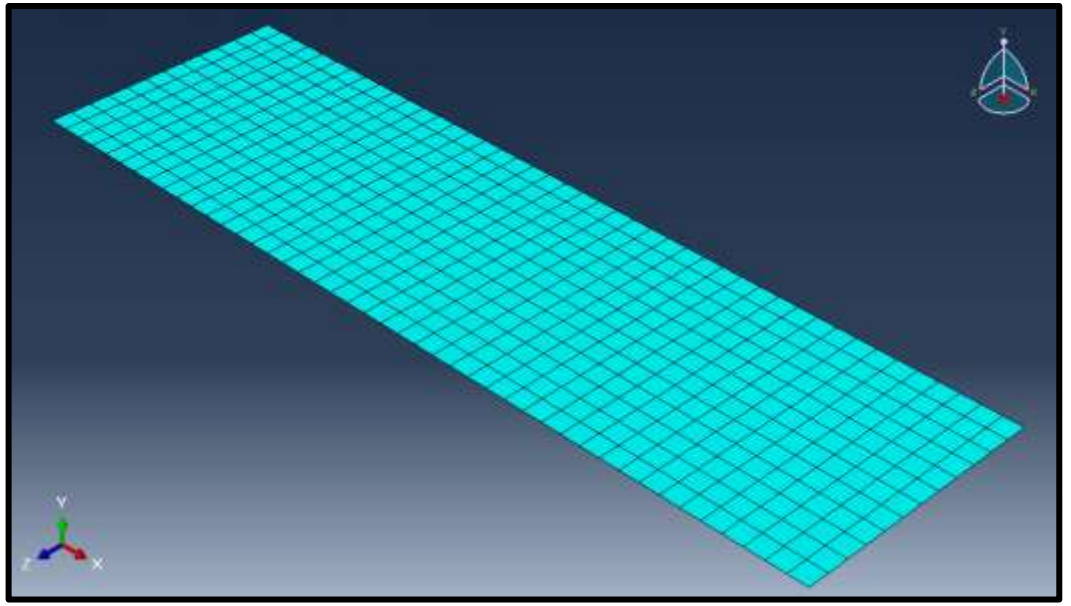


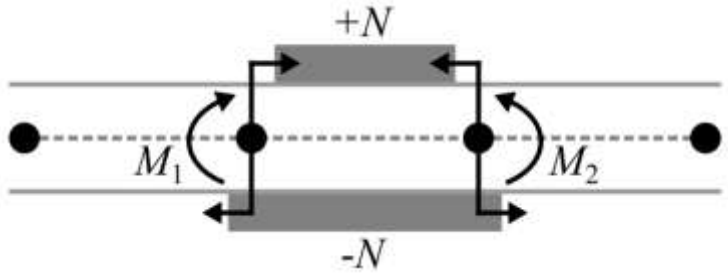
REDUCED-ORDER MODELING OF SHOCKED PCBS

Fast models capture the dominant dynamics needed for control design.

- Beam models represent the dominant PCB bending response
- Piezoelectric patches are represented as localized moment couples
- Predictions are validated against higher-fidelity shell models
- Reduced order enables rapid simulation and control development



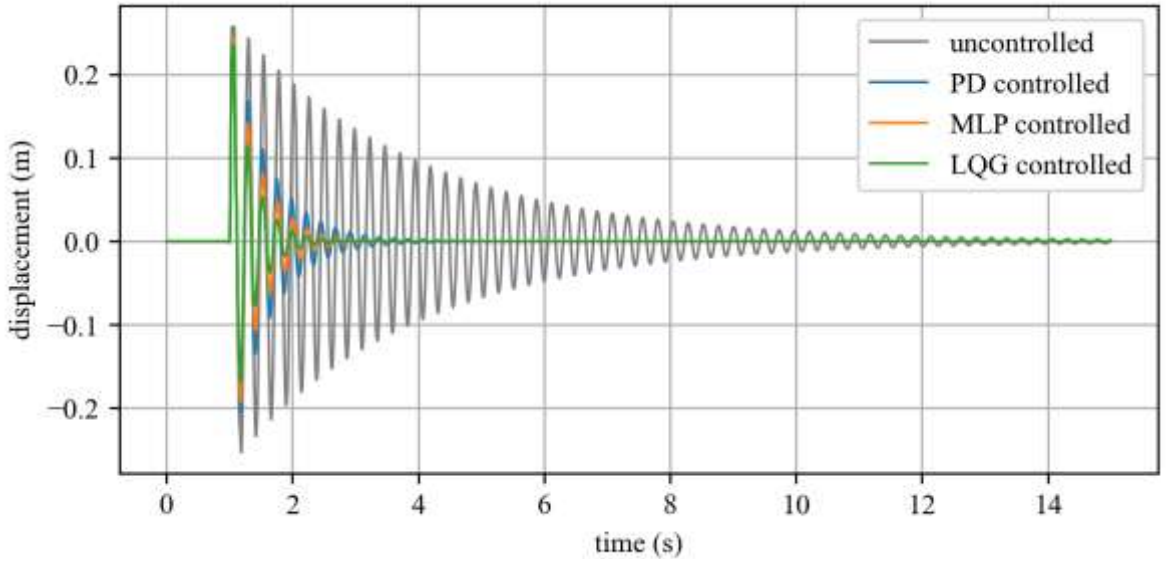


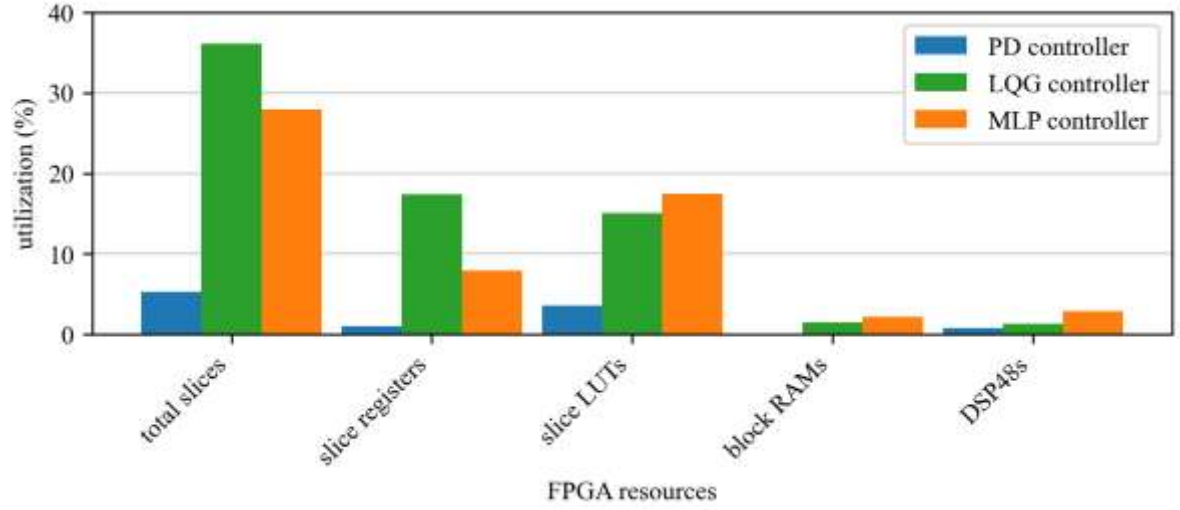


FPGA-BASED ACTIVE CONTROL

Ongoing work compares embedded controllers for rapid vibration suppression.

- PD, LQG, and MLP controllers are deployed on FPGA hardware
- Controller performance and FPGA resource use are benchmarked
- Learning-based control can reduce hardware cost while maintaining damping performance
- Supports future low-latency active mitigation of shock response



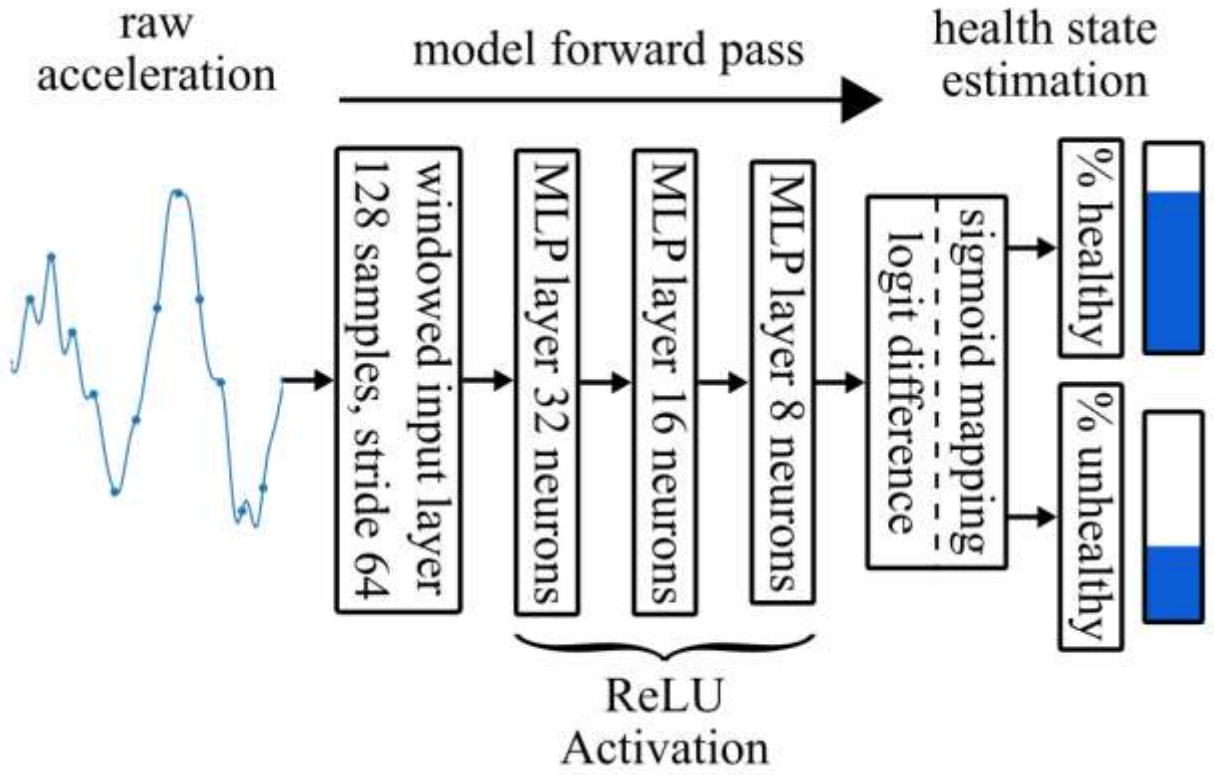


FOCUSED STUDY

OBJECTIVE

Develop and evaluate an FPGA-deployed MLP for high-rate PCB health-state estimation from shock-response acceleration. The model must provide:

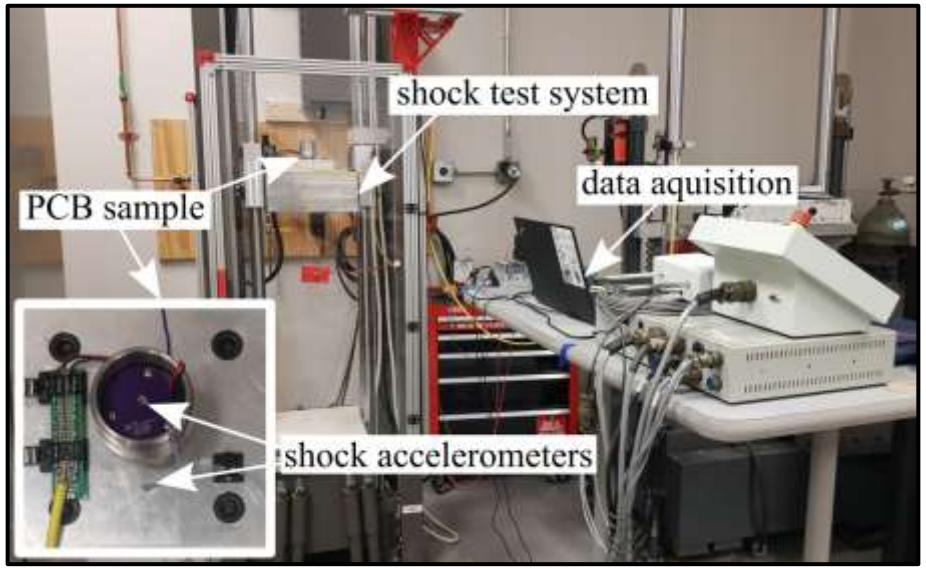
- Accurate impact-level classification
- Deterministic, sub millisecond inference
- Effective FPGA resource utilization

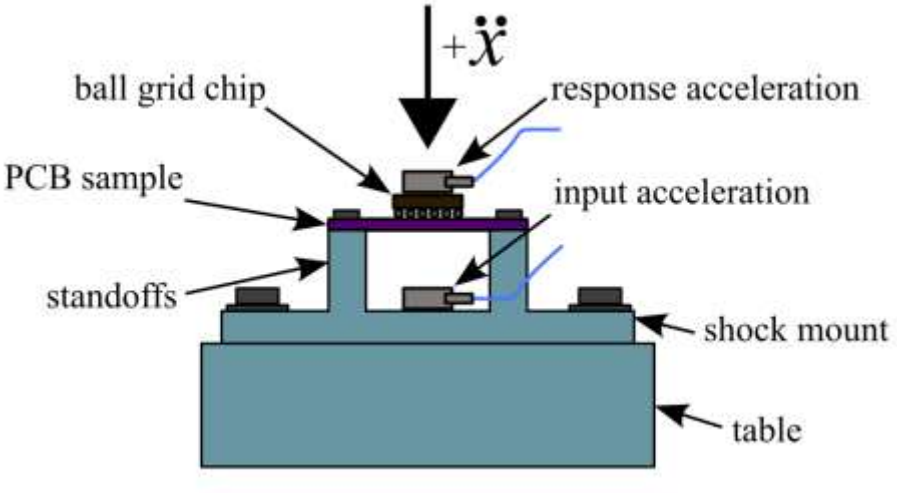


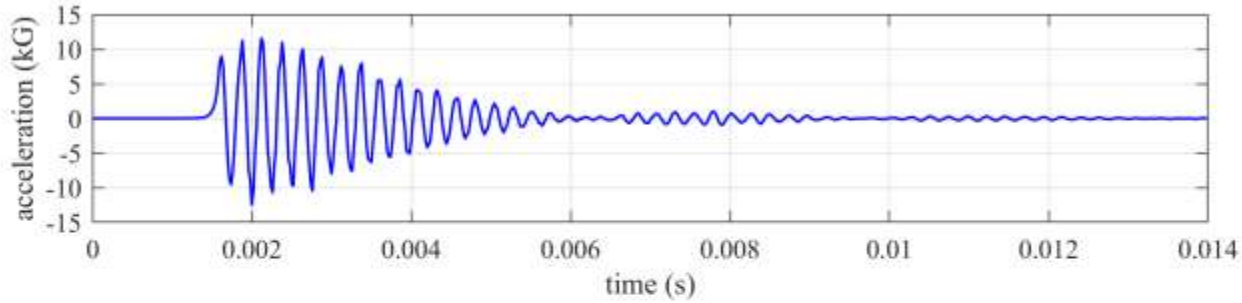
EXPERIMENTAL DATASET

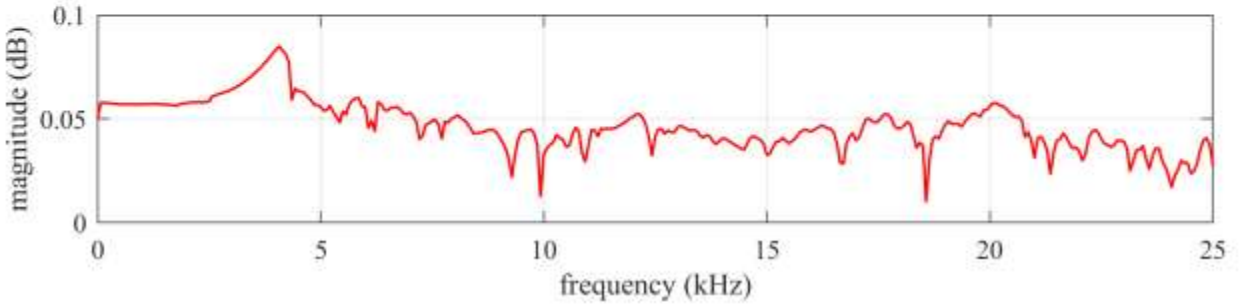
PCB response acceleration was measured during controlled repeated-shock testing.

- 30 controlled impacts, sampled at 51.2 kS/s
- Average response: 10,000 g_n, 322 μs half-sine duration
- ≈ 4 kHz dominant PCB resonance





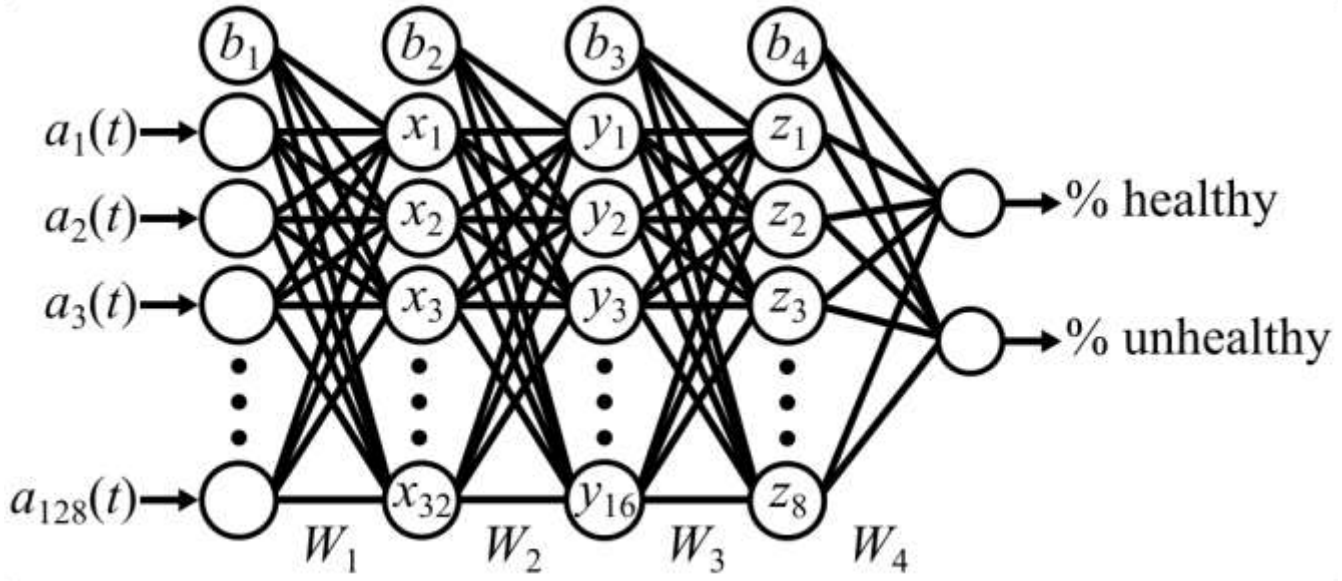




MODEL ARCHITECTURE

A compact MLP maps each acceleration window to a health-state estimate.

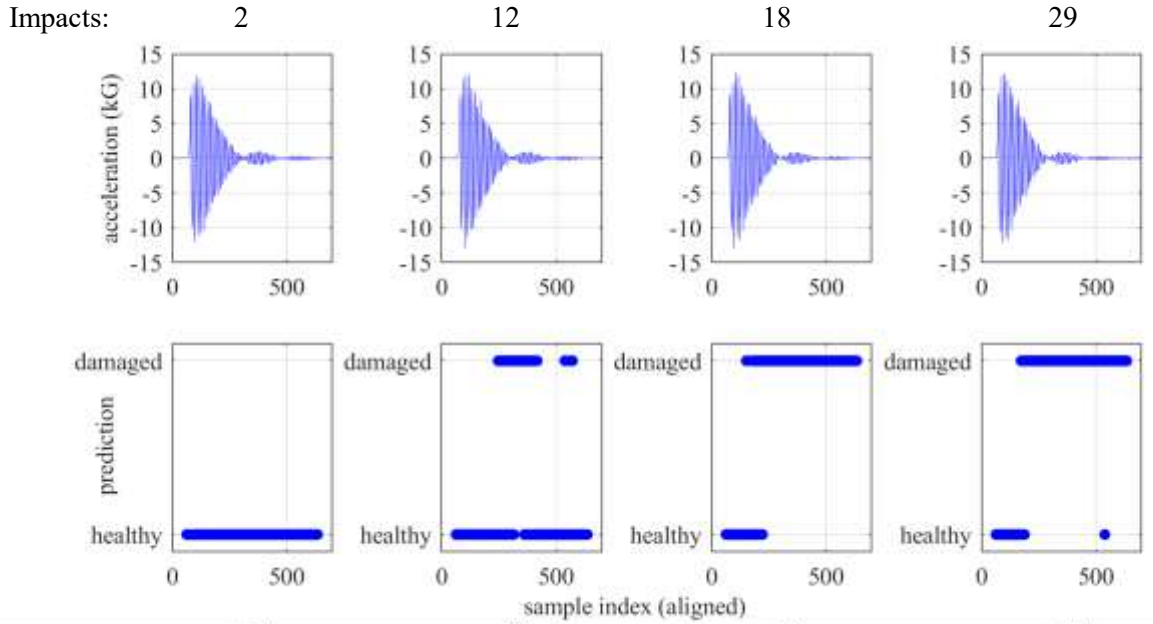
- 128-sample acceleration windows with a stride of 64 samples
- Three hidden layers with 32, 16, and 8 neurons; ReLU activation after each hidden layer
- The output-logit difference is mapped through a sigmoid to estimate unhealthy-state probability

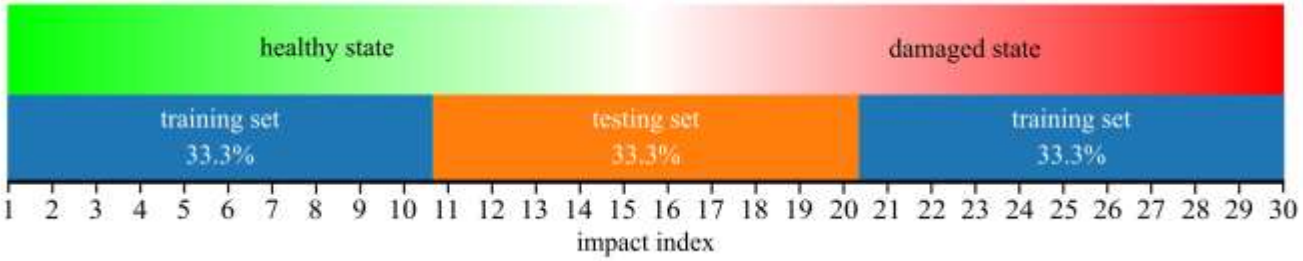


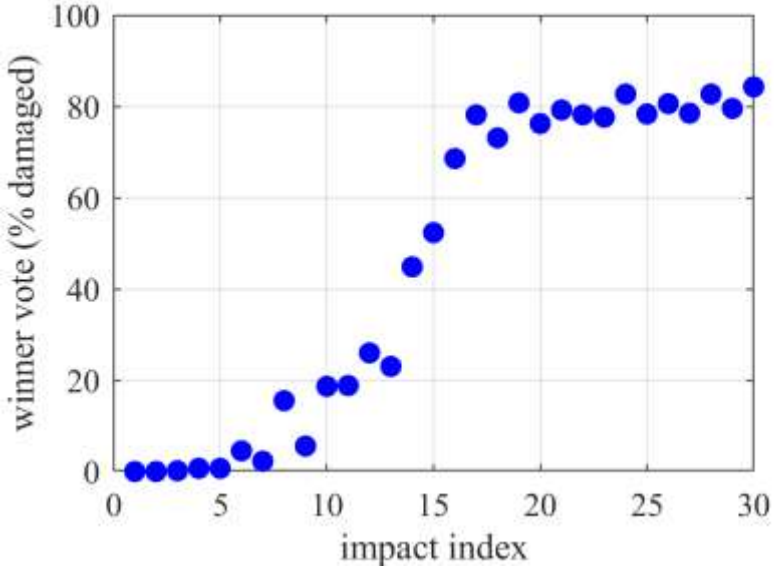
MODEL TRAINING

The MLP was trained offline using chronologically separated impact events.

- Train: first 10 healthy + final 10 damaged impacts
- Validate: middle 10 impacts
- Acceleration traces were aligned to the PCB-response peak and trimmed to a fixed length
- Adam optimization with mini-batch updates and early stopping
- Dropout in the first two hidden layers during



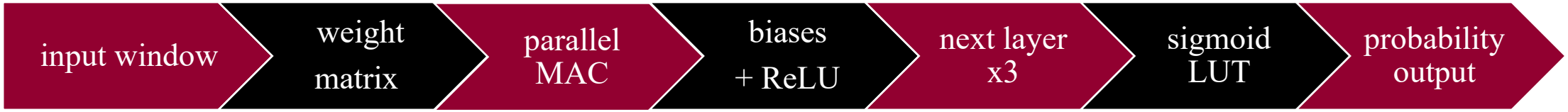




FPGA IMPLEMENTATION

The FPGA executes one bounded MLP forward pass per input window.

- Transposed weights and biases are stored in on-chip BRAM
- Fully connected layers use parallel multiply-accumulate operations
- ReLU activations are stored and passed to the next layer
- A 512-entry sigmoid lookup table returns the unhealthy-state probability



Fixed arithmetic and memory-access sequences produce deterministic per-window execution.

PERFORMANCE

The deployed MLP achieved accurate classification with deterministic FPGA inference.

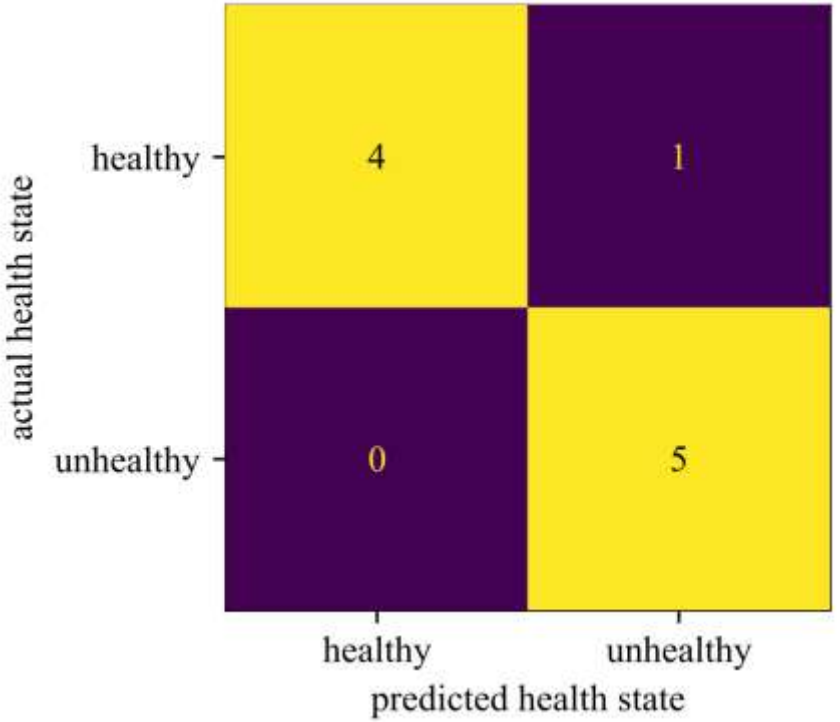
Model:

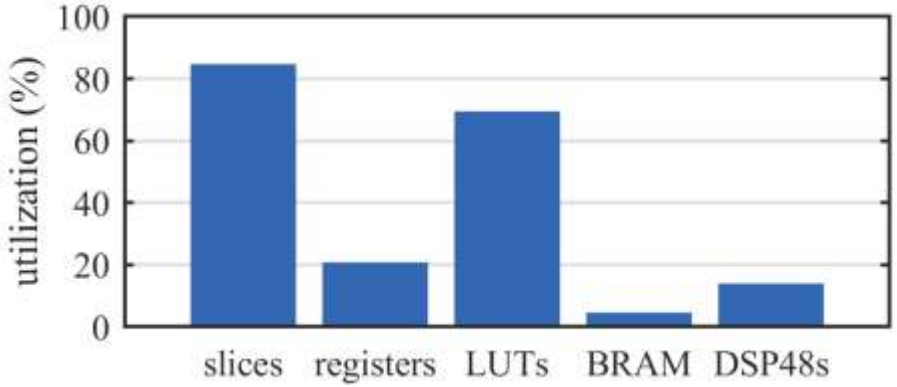
- **90%** impact-level validation accuracy

Hardware:

- **<u>0.609 ms</u>** per 128-sample window at 40 MHz
- Resource use is dominated by slices and LUTs

	slices	registers	LUTs	BRAM	DSP48s
utilized	21479	42230	70488	15	84
total	25350	202800	101400	325	600
percent	84.7%	20.8%	69.5%	4.6%	14.0%

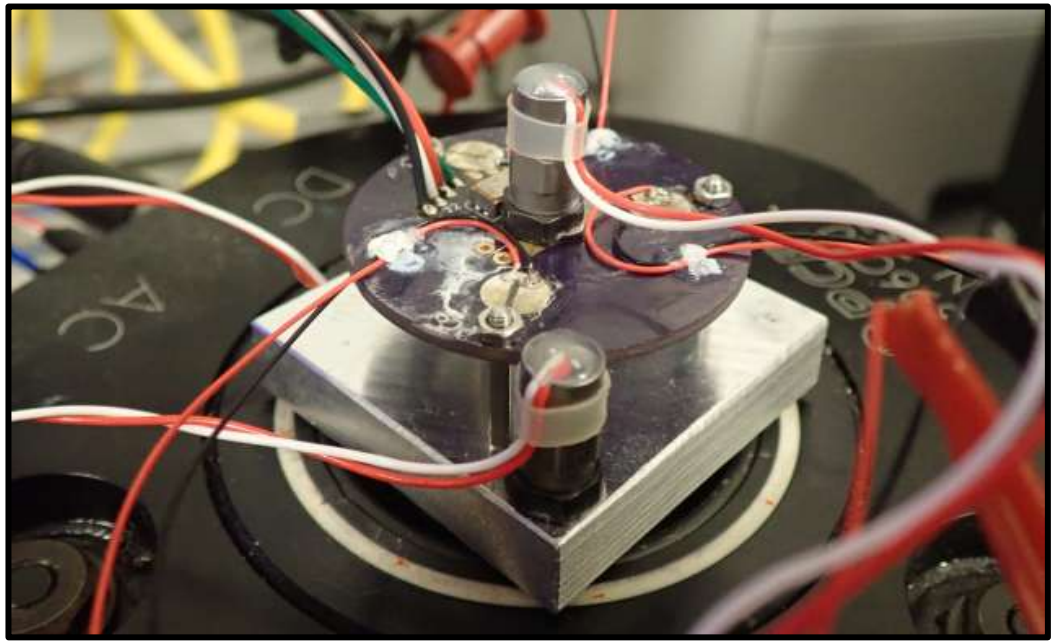




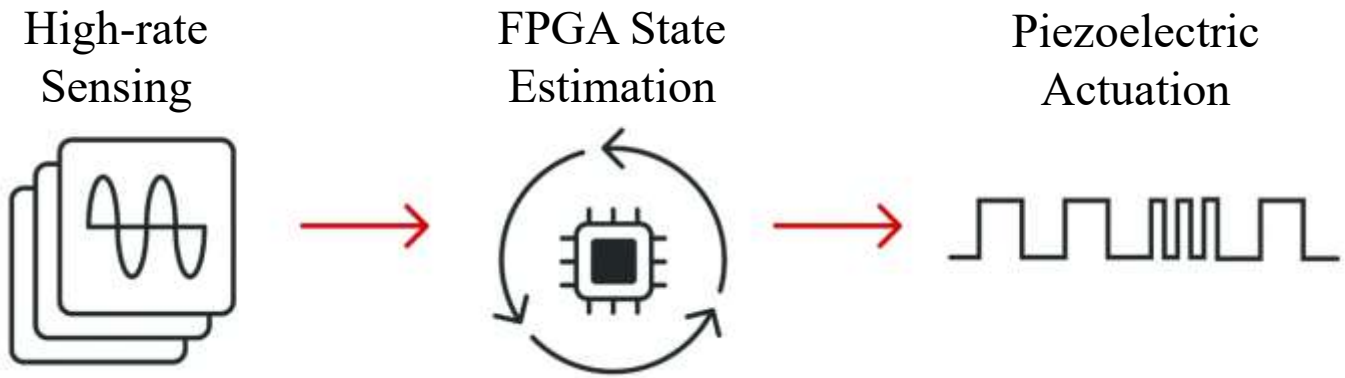
FUTURE WORK

The long-term objective is to use state-aware control to reduce damaging PCB response.

- Measure high-rate structural response and damage progression
- Estimate state on embedded FPGA hardware
- Drive piezoelectric actuators to mitigate damaging vibration and shock response



PZT Actuator Patches



QUESTIONS?

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EXTENDED WORK

- Extended dataset to 150 controlled impacts (more data to train/validate)
- Xilinx matrix multiply implementation (15.9 μs)