FPGA-Deployable Approximate Topological Framework for Low-Latency Change-Point Detection in PCB Shock and Vibration Response

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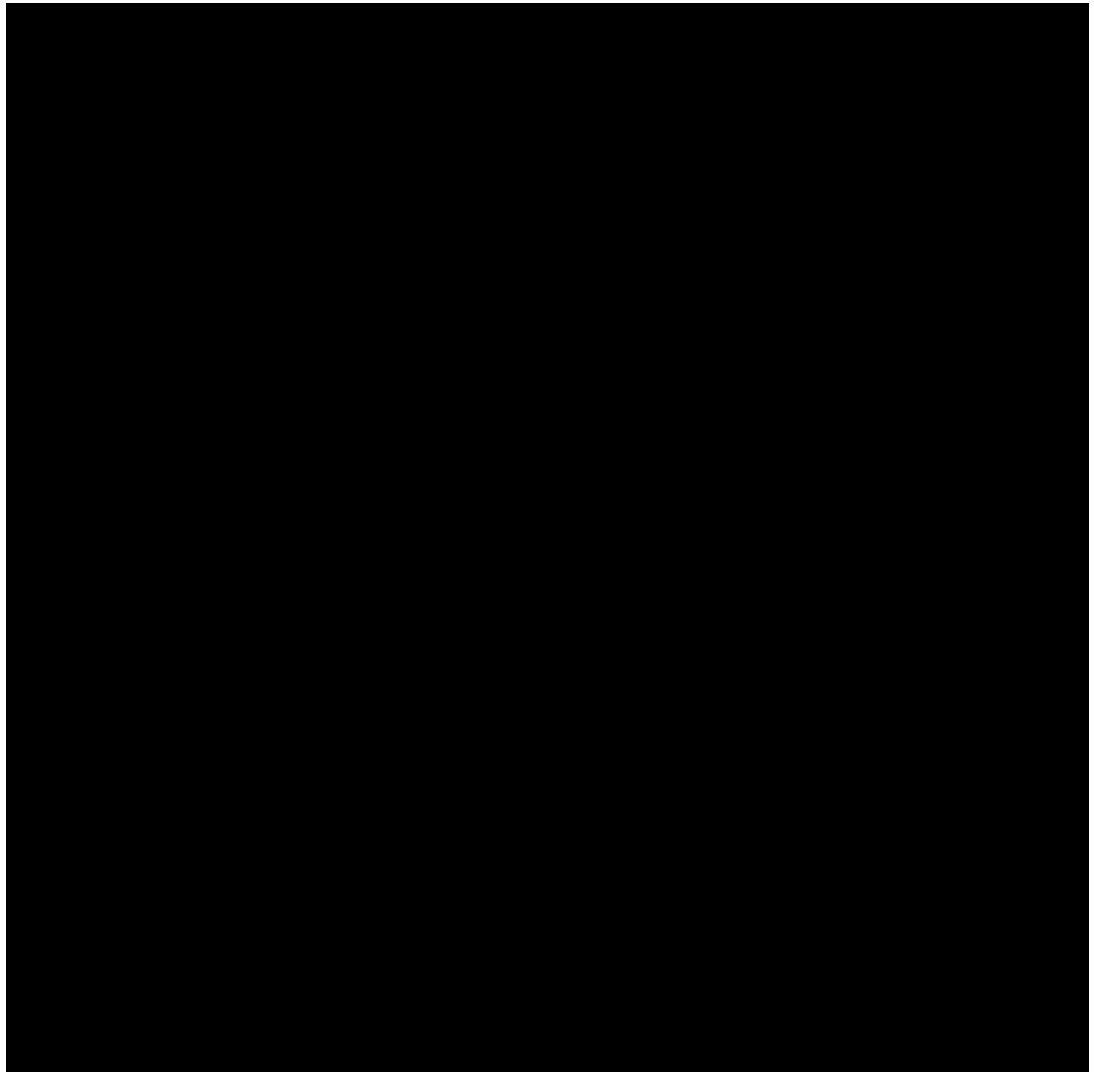
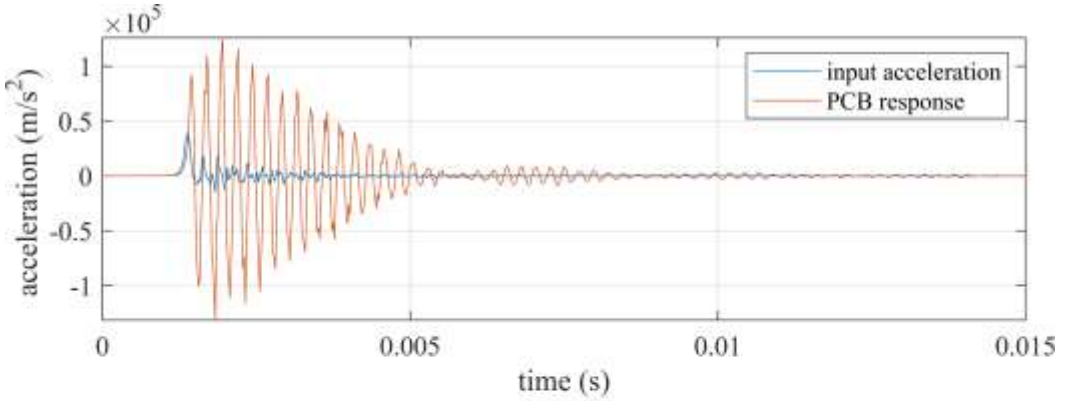
High-Rate Dynamics

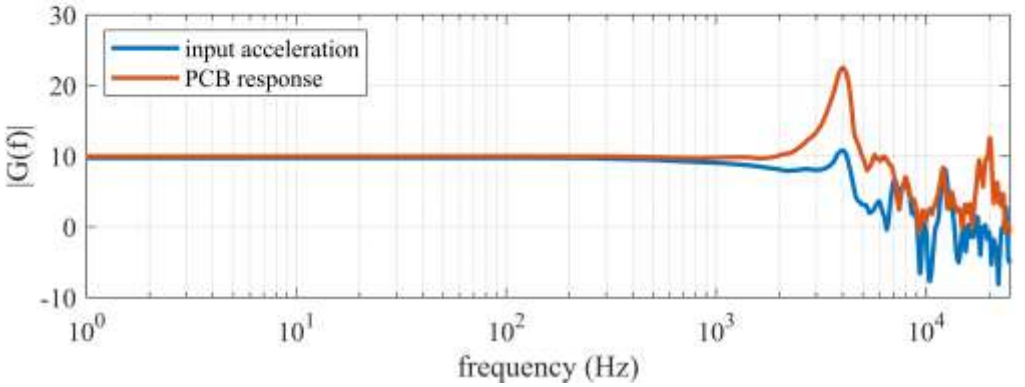
- High-rate dynamics are structural responses to high-amplitude events occurring in less than 100 ms, typically exceeding 100 g, such as blast or impact.
- They are characterized by:
  - Large uncertainty in the external load
  - Strong nonstationarity and disturbances in the structure
  - Previously unmodeled dynamics as the system configuration changes
- Decision-latency regimes:
  - High-rate: 1 ms
  - Very high-rate: 100 μs
  - Ultra-high-rate: 1 μs

Jacob Dodson, Austin Downey, Simon Laflamme, Michael Todd, Adriane G. Moura, Yang Wang, Zhu Mao, Peter Avitabile, and Erik Blasch. High-Rate Structural Health Monitoring and Prognostics: An Overview. Data Science in Engineering, Volume 9, Proceedings of the 39th IMAC, A Conference and Exposition on Structural Dynamics 2021, Springer International Publishing, p. 213-217, Oct 2021. doi:10.1007/978-3-030-76004-5_23

Shock Testing our North Star System





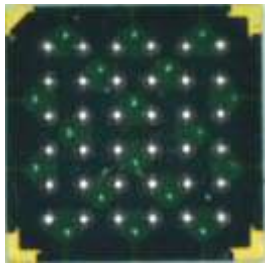


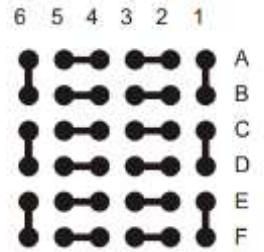
Dataset

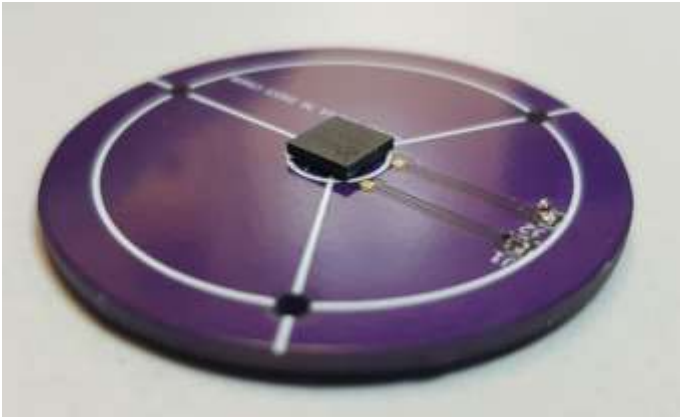
https://github.com/High-Rate-SHM-Working-Group/Dataset-5-Extended-Impact-Testing/tree/main/data/dataset-2

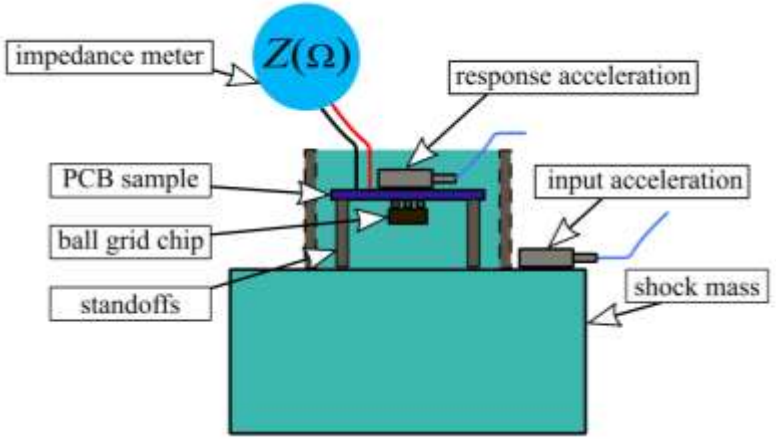
Experimental System (North Star)

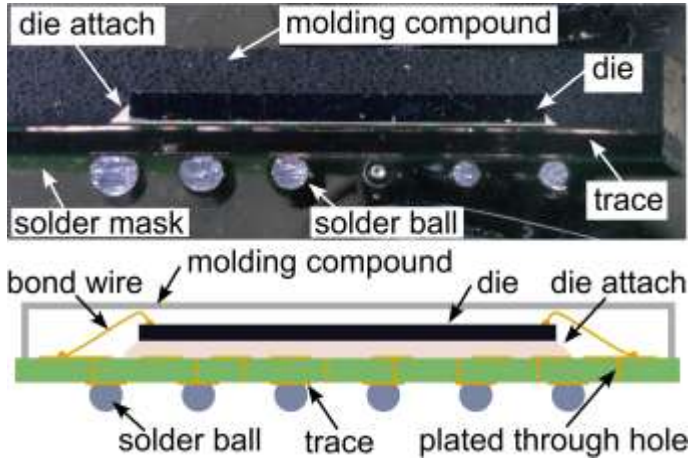
- Stiff circular PCB provides a controlled, repeatable test article
- Ball-grid-array package represents a realistic electronics interconnect
- High-rate shock loading drives the board and package response
- Measure input and local response acceleration during each event
- Track electrical impedance to link mechanical shock with functional damage





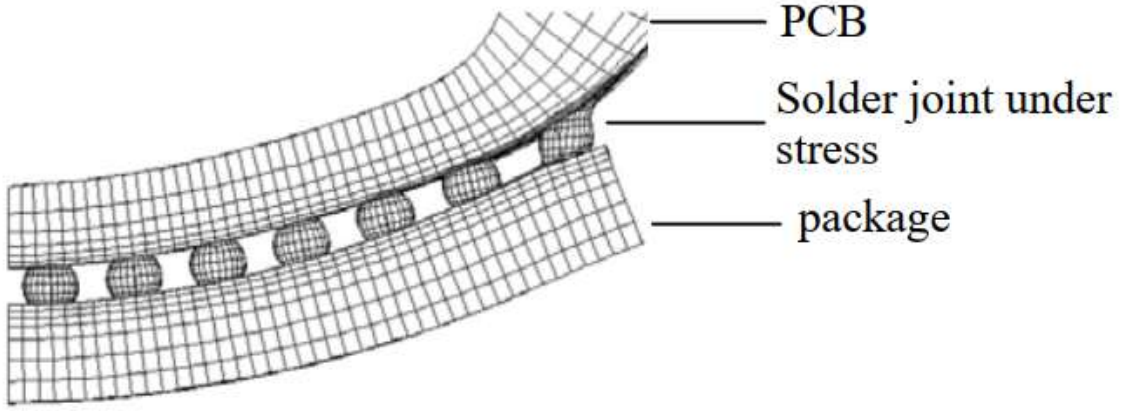




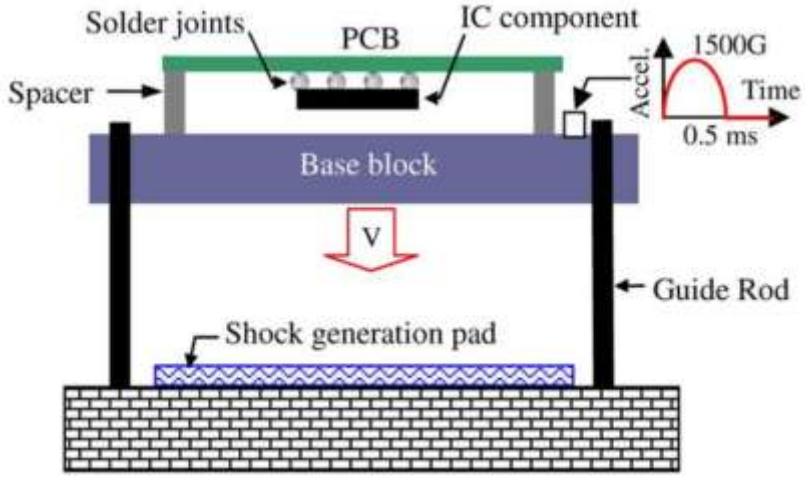


PCB Failure Mechanisms under Shock

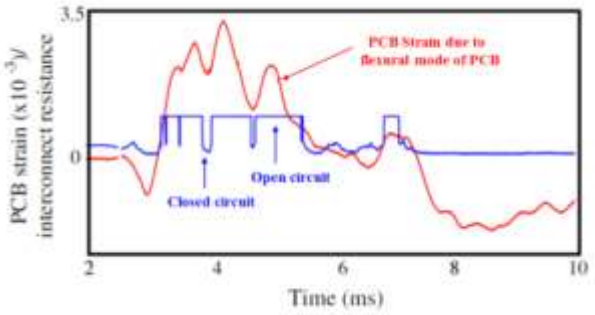
- PCB failures under shock are caused by:
  - Bending of the base PCB board, causing stresses to build up at the solder balls.
  - Adhesion challenges of masses (components) accelerating away from the PCB.

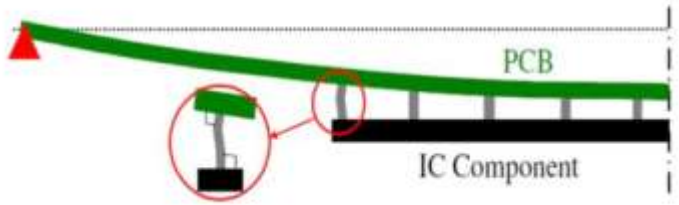


Seah, S. K. W., Wong, E. H., Ranjan, R., Lim, C. T., and Mai, Y. W., 2005, "Understanding and testing for drop impact failure," ASME Pacific Rim Technical Conference and Exhibition on Integration and Packaging of MEMS, NEMS, and Electronic Systems, pp. 1089-1094.



Wong, E. H., Yiu-Wing Mai, and Matthew Woo. "Analytical solution for the damped-dynamics of printed circuit board and applied to study the effects of distorted half-sine support excitation." IEEE Transactions on advanced packaging 32.2 (2009): 536-545.



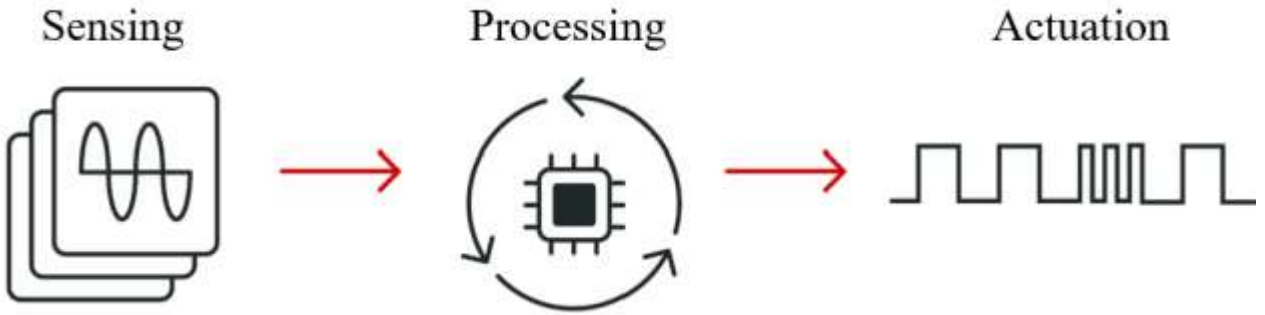


Chen, Zhuo. *Effective Mitigation of Shock Loads of Embedded Electronics in Smart Ammunitions by Polymeric Encapsulation*. Diss. University of Toronto (Canada), 2014.

How to Close the Loop from Monitoring to Control?

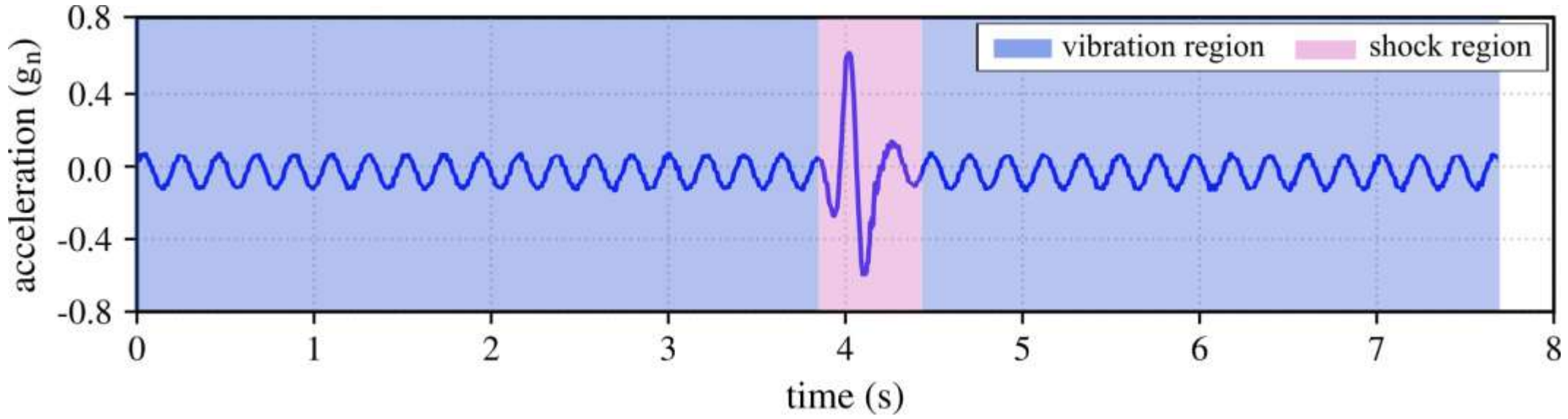
Active control of the structural deflection of electronics could:

- Increase their survivability
- Increase their serviceability
- Open them up to new applications
- Reduce their packaging constraints
  - Size
  - Weight
  - Thermals



Real-Time Shock and Vibration Detection

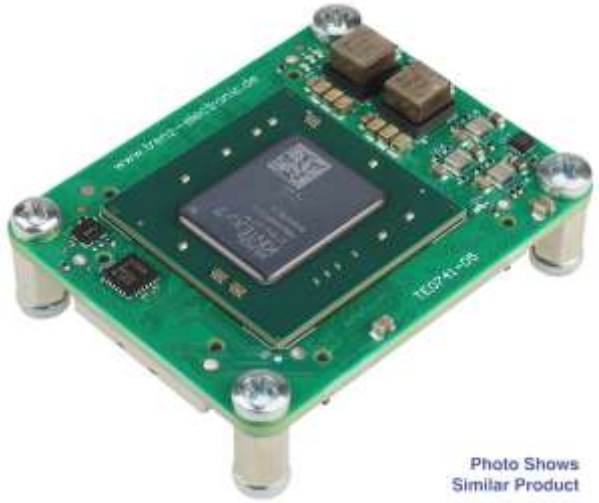
- Vibration and shock create different failure risks and require different control actions.
- Sustained vibration drives fatigue damage, so the controller should reduce ongoing response.
- Shock can cause fracture, so the controller must anticipate the event and limit peak amplitude.
- The system must identify shock versus vibration fast enough to select the appropriate controller.
- Detection must run efficiently on embedded hardware with limited computation and memory.



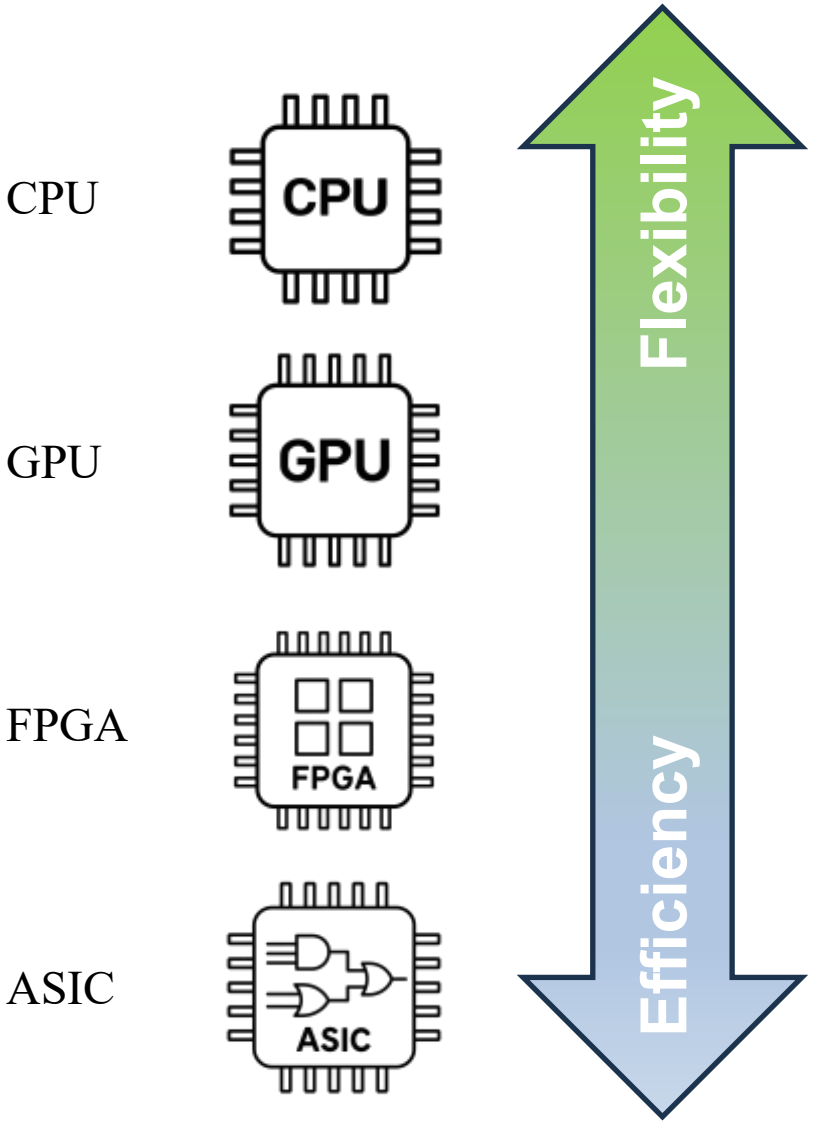
WHY AN FPGA?

Field programmable gate arrays (FPGA) map a fixed model into dedicated hardware for predictable embedded inference.

- CPU/GPU execution is flexible, but timing can vary
- ASICs are efficient, but fixed-function and costly to redesign
- FPGAs provide reconfigurable hardware with bounded latency
- On-chip memory keeps model parameters close to computation
- Hardware parallelism can be tailored to the model architecture



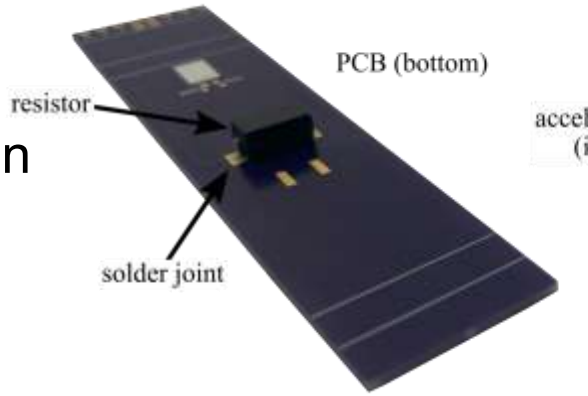
Kintex-7 K70T-2C

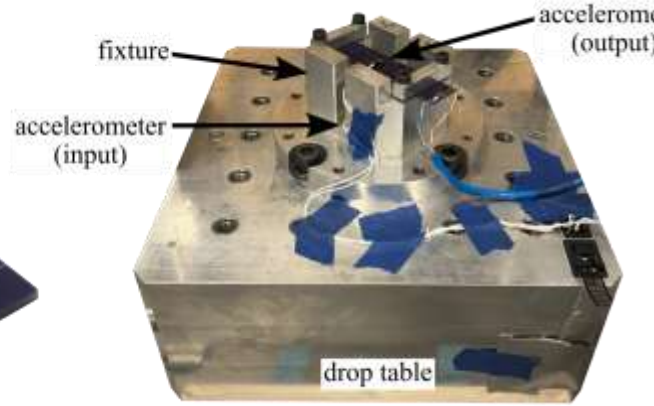


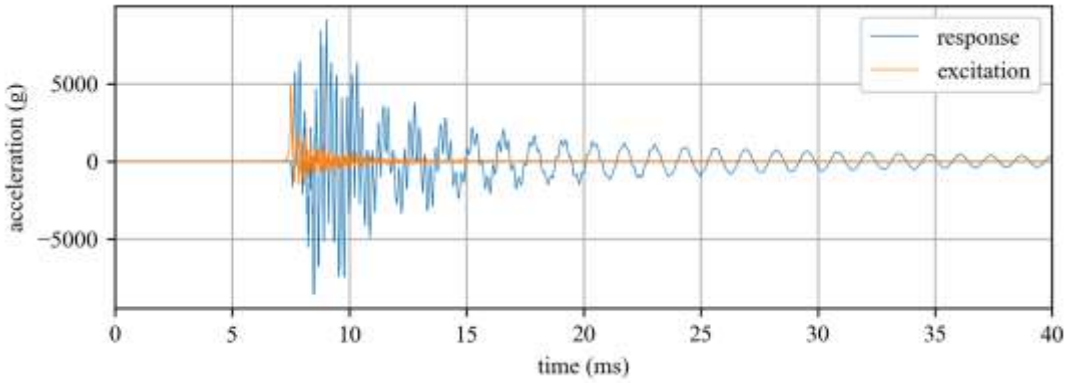
Our Relevant Prior Work

Test-to-Failure Dataset Development

- Printed circuit boards mounted as fixed–fixed beams with a surface-mount resistor at midspan
  - 175Tg FR4
  - 25.40 × 76.20 × 1.60 mm
  - 100 mΩ, 1 W resistor
- Subjected to repeated shock loading at constant impact energy
  - 5000 g and 0.2 millisecond pulse duration (9.8 m/s is a moderate car crash)
  - 12-inch drop using bungees, 1/16th inch felt
- Acceleration measured at the fixture and board midspan to capture input–response behavior.



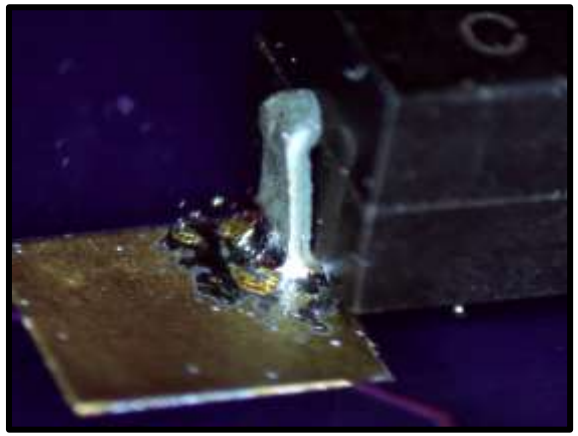


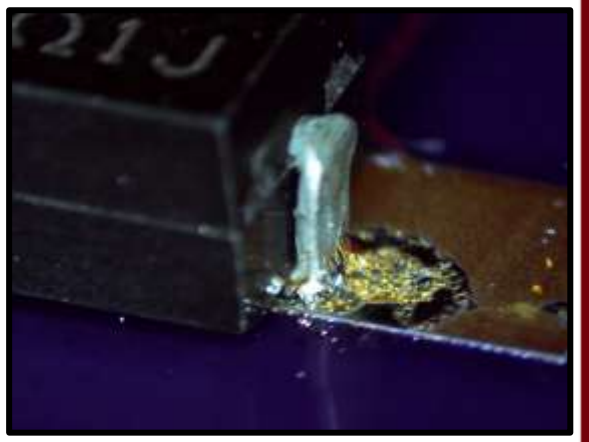


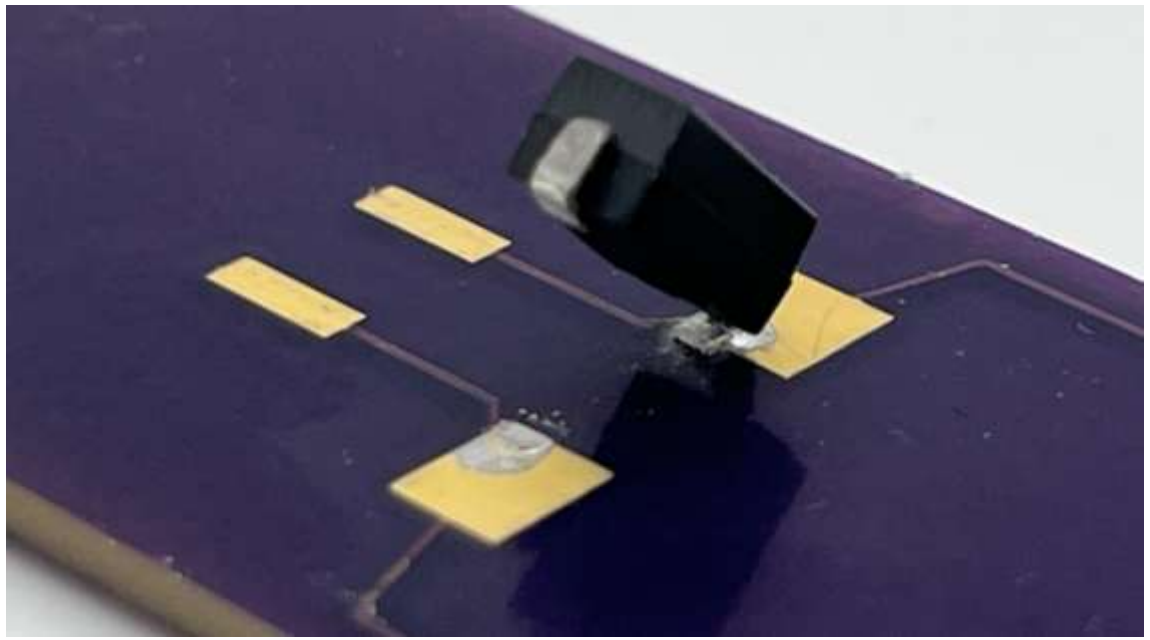
Trotter Roberts, Hugo Luck, Joud N. Satme, Mohsen Gol Zardian, Sina Navidi, Ryan Yount, Austin R. J. Downey, and Chao Hu. Test-to-failure characterization and acceleration signal feature analysis of electronic systems under repeated shock loading. In Proceedings of the Society for Experimental Mechanics (SEM) IMAC Conference, 2026

System Failure

- Repeated high-g impacts cause crack initiation and growth in solder joints connecting surface-mount resistors.
- Resistor eventually lifted or detached as solder joints fractured.
- PCB substrate remained intact; failure isolated to solder fatigue.
- Consistent failure mode observed across all tested boards.



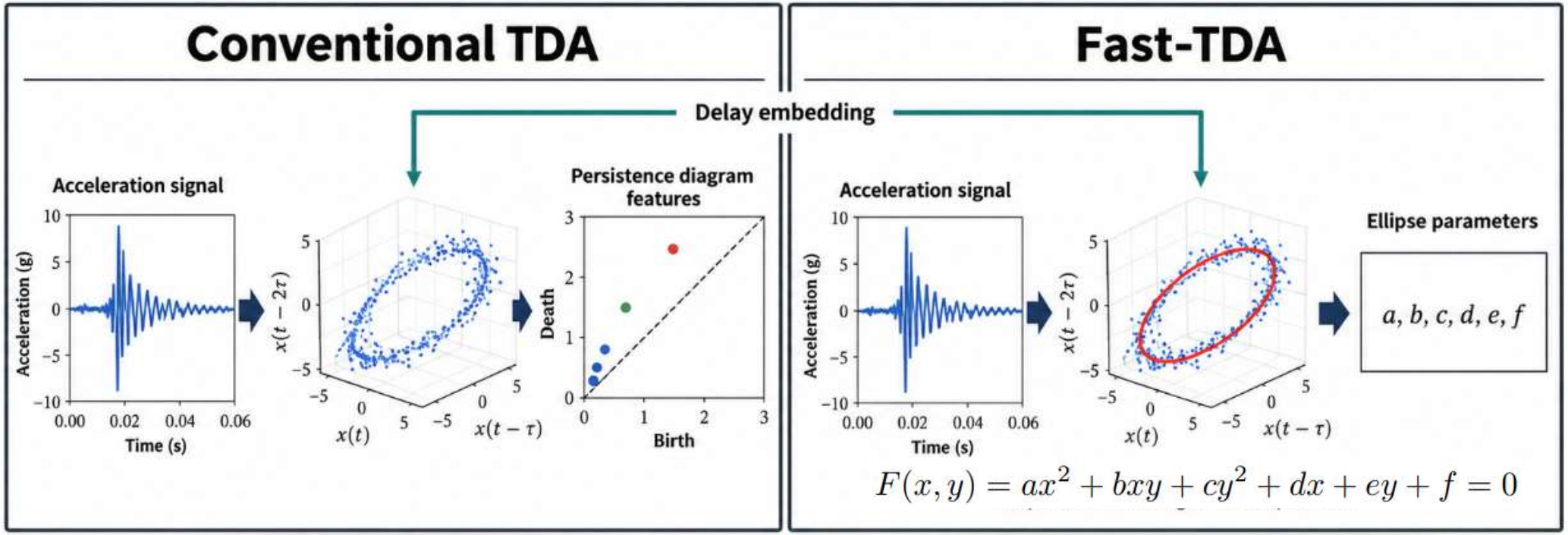




Current Work

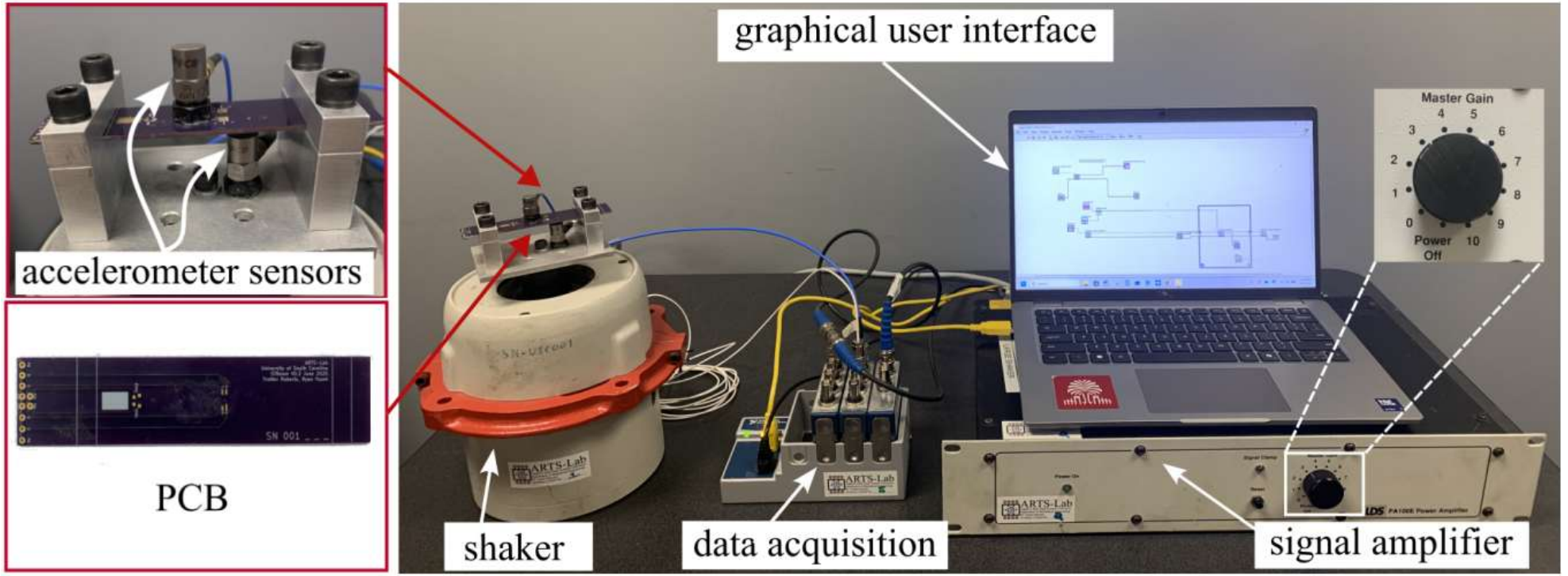
Fast Topological Data Analysis (FTDA)

- Conventional TDA computes persistence diagrams repeatedly.
- Fast-TDA uses ellipse fitting as an approximate geometric feature.



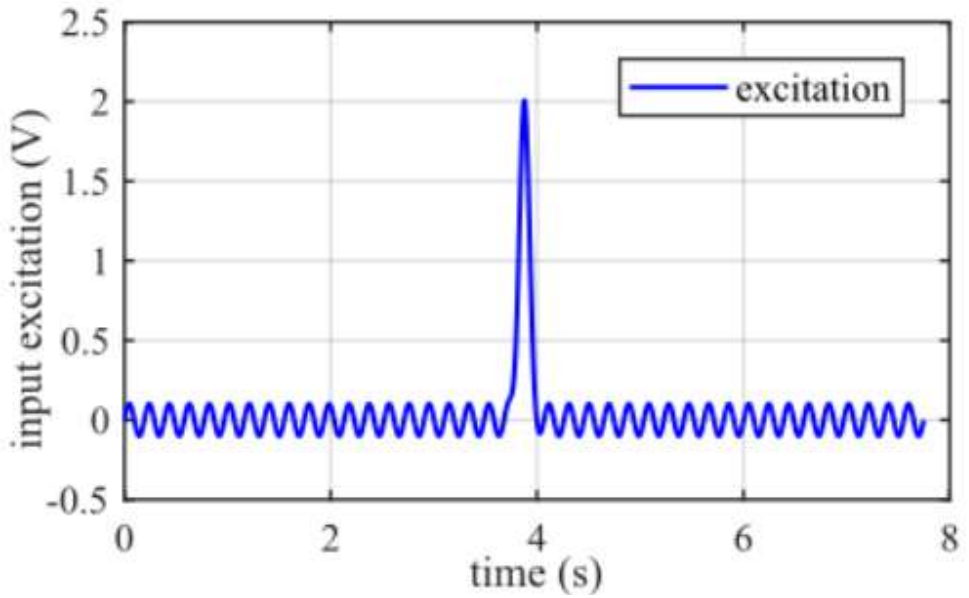
Experimental Setup and Data Acquisition

- A fixed-fixed PCB was mounted on an electrodynamic shaker
- LabVIEW generated the voltage excitation.
- An amplifier drove the shaker.
- Accelerometers measured the PCB response synchronously.

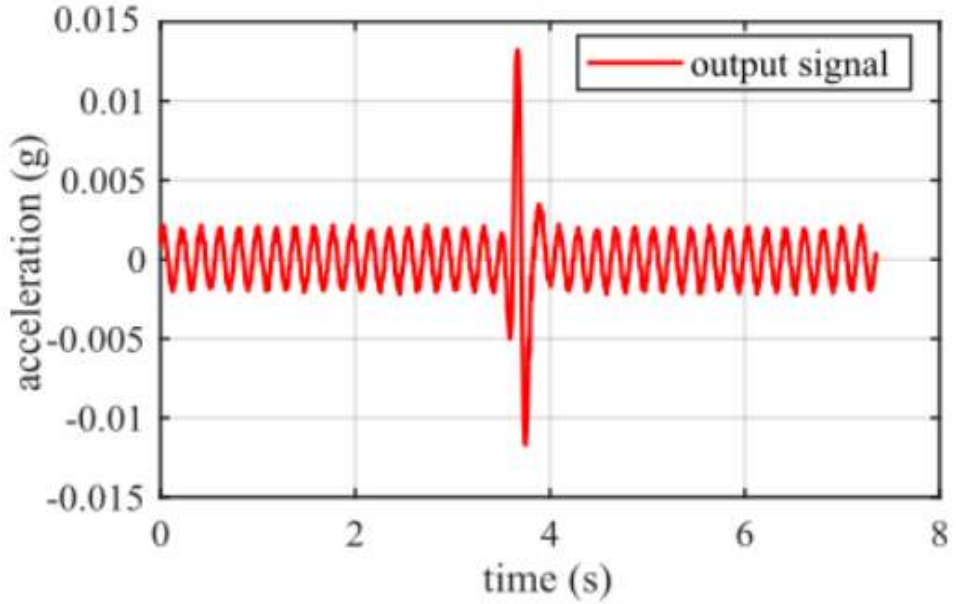


PCB Response Under Combined Vibration and Shock

- Harmonic vibration provides the baseline excitation.
- A single impulsive shock is introduced during the test.
- The measured acceleration shows a sharp transient at shock onset.



Combined harmonic with shock signal

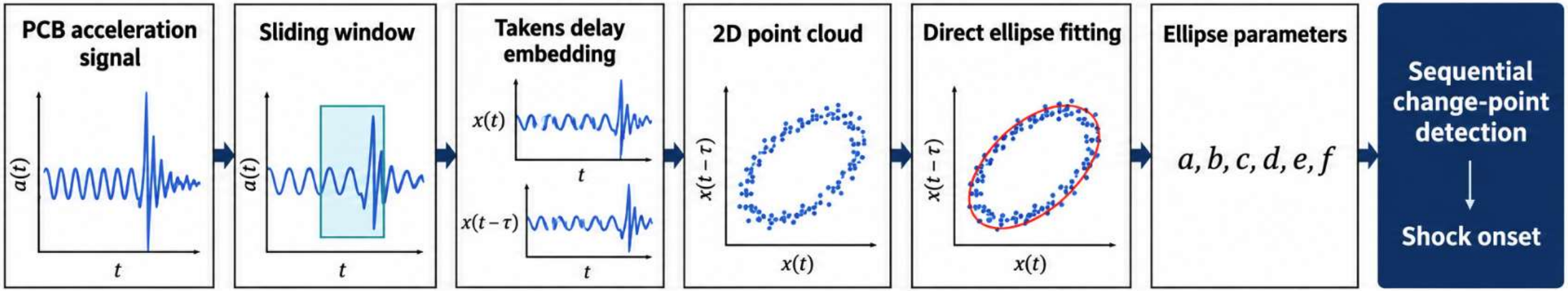


Vibration response

Fast-TDA Shock Detection Framework

- The acceleration signal is processed in sliding windows.
- Delay embedding creates a two-dimensional point cloud.
- Ellipse parameters become monitoring features for change-point detection.

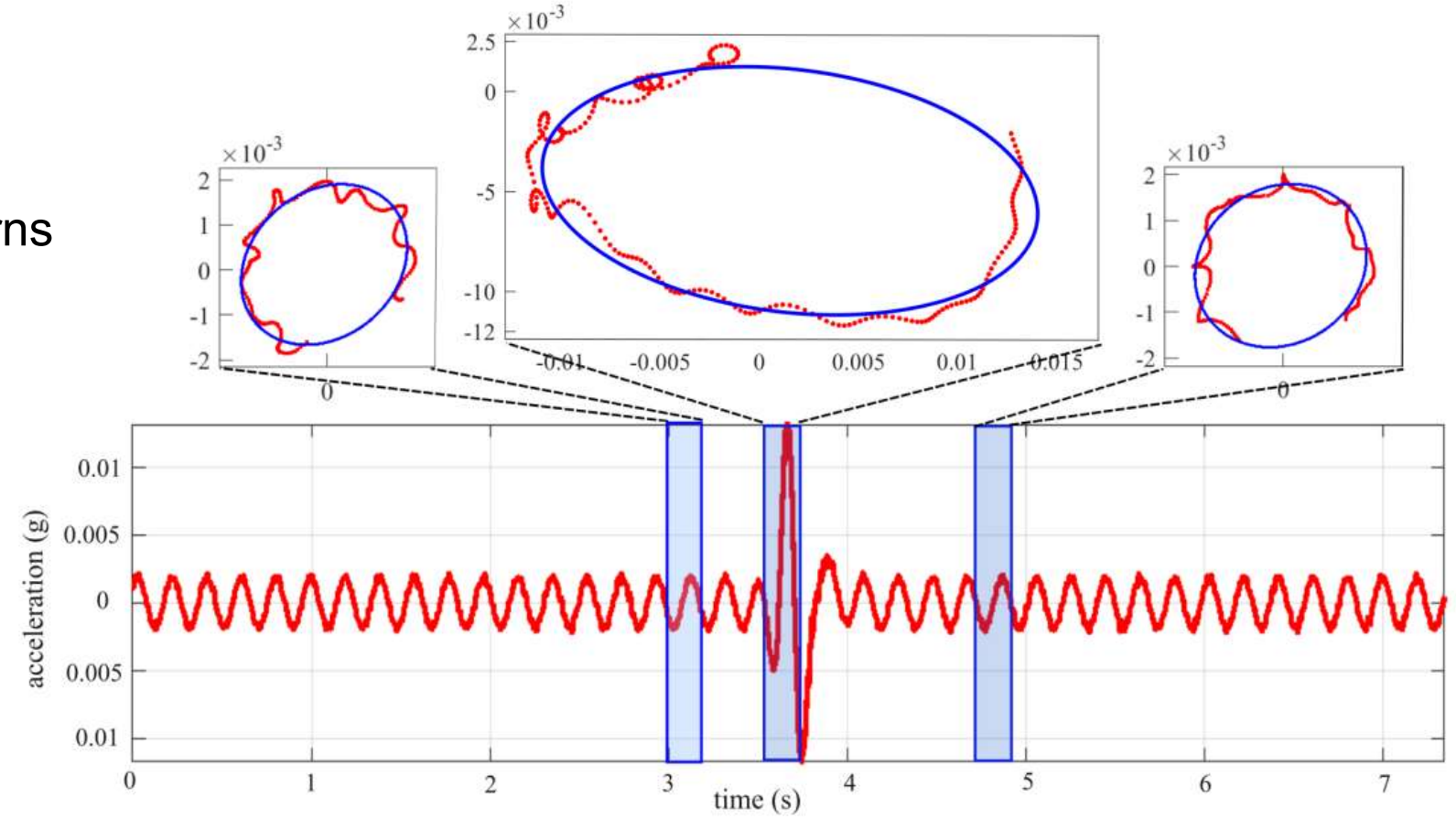
$$F(x, y) = ax^2 + bxy + cy^2 + dx + ey + f = 0$$



Shock detection framework

Geometric Response of the Delay-Embedded Point Cloud

- Before shock, the point cloud forms a compact orbit.
- During shock, the fitted ellipse elongates and rotates.
- After shock, the geometry returns toward its steady pattern.



pre-shock, shock, and post-shock

Signal to Point Cloud Mathematical Derivation

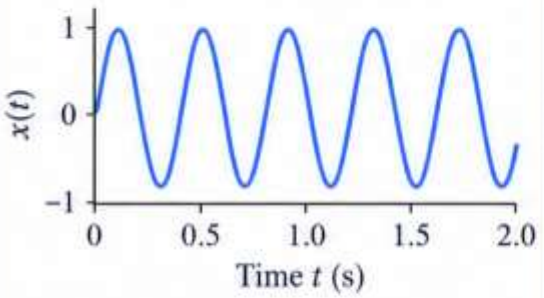
Measured PCB acceleration provides the input signal for each Fast-TDA window.

The delay uses one quarter of the dominant period. The window length uses one period of the lowest frequency.

Zero padding makes the earliest delayed windows valid before the original signal begins.

Each sample pairs with its delayed copy to form the two-dimensional point cloud used for ellipse fitting.

Acceleration signal $x(t)$



$$x[n] = x(n\,\Delta t)$$

Delay and window length

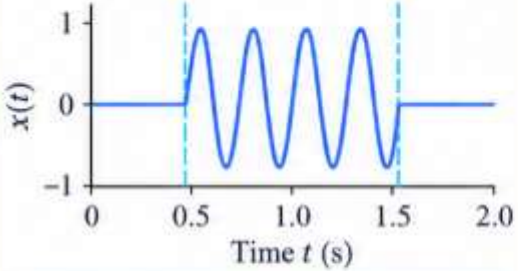
$$\text{delay} = 0.25 / F_{\max}$$

$$\text{window length} = 1 / F_{\min}$$

$$d = \text{round}(\text{delay} / \Delta t)$$

$$N_w = \text{round}(\text{window length} / \Delta t)$$

Zero-padded sliding window

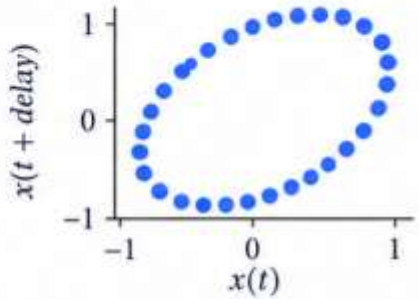


$$N_{\text{pad}} = N_w - 1 + d$$

$$x_{\text{pad}}[n] = 0,\ n < N_{\text{pad}}$$

$$x_{\text{pad}}[n] = x[n - N_{\text{pad}}],\ n >= N_{\text{pad}}$$

Takens embedding



$$P_i = \{\,[x(i+k),\, x(i+k+d)]\,\}$$

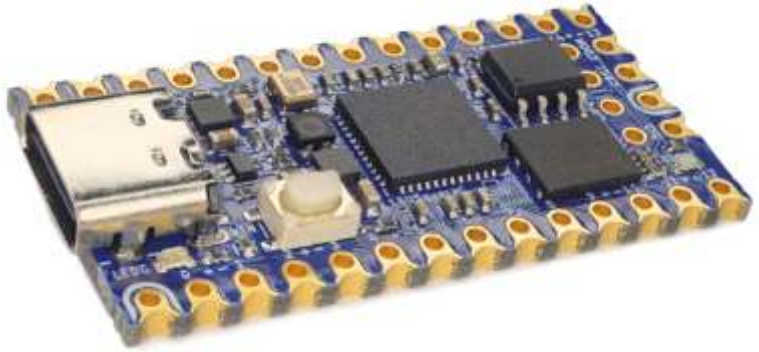
$$k = 0, \ldots, N_w - d - 1$$

$$P_i \in \mathbb{R}^{(Nw-d)\times 2}$$

Quick Primer on FPGAs

Field Programable Gate Array

- A Field-Programmable Gate Array (FPGA) is a reconfigurable hardware device, making it ideal for real-time applications.
- Low-latency processing for rapid control adjustments.
- Custom hardware acceleration for ML and structured controllers.



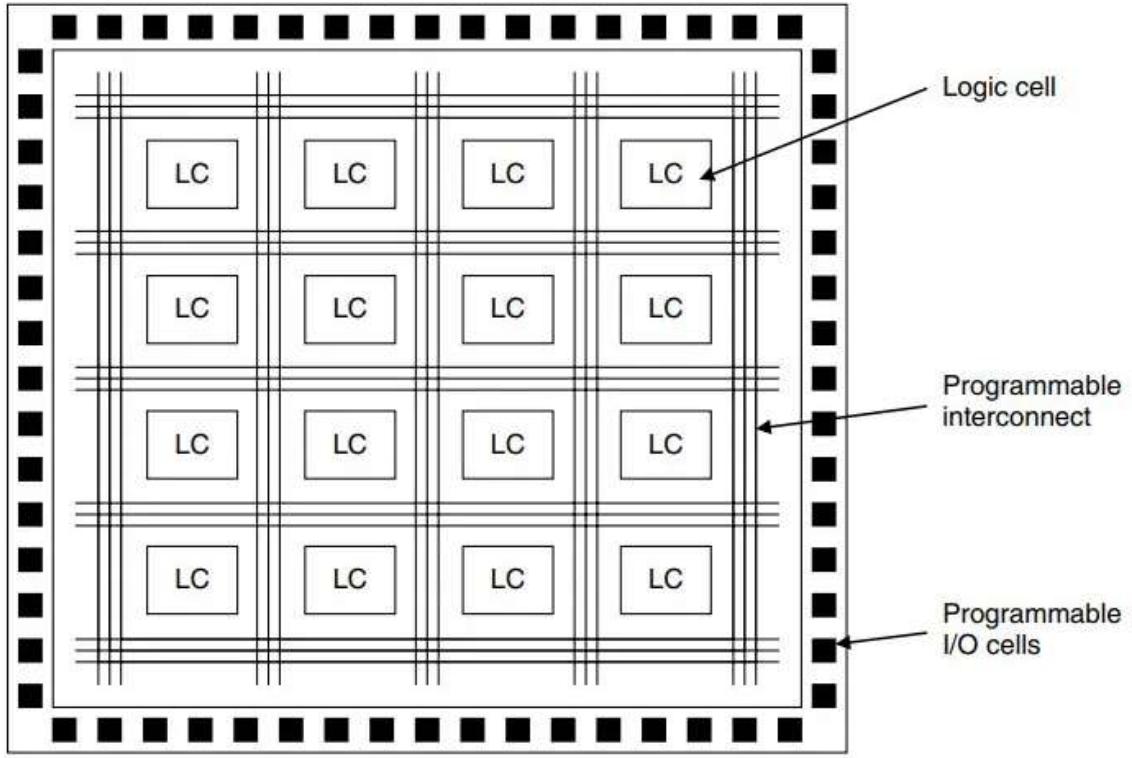
ICE40

Kintex-7 K70T-2C

U55C UltraScale+

FPGA Components

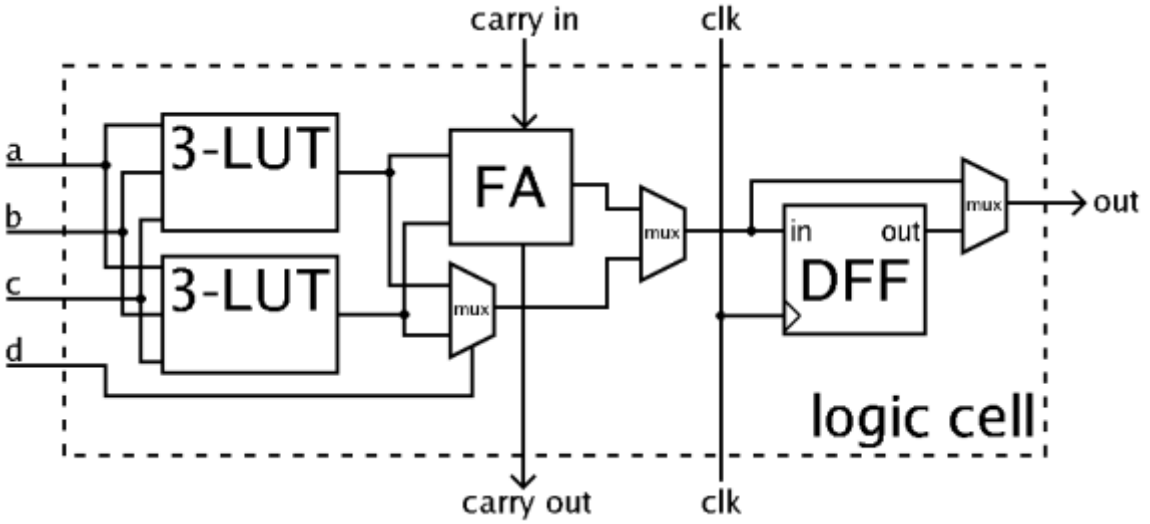
- Typically, an FPGA consists of three basic components:
  - Programmable Logic Cells/Blocks (also called slices)
  - Programmable Routing
  - IO Blocks
- Logic Blocks are responsible for implementing the core logic functions.
- Routing is responsible for connecting the Logic Blocks.
- IO Blocks are connected to the Logic Blocks through the routing and help to make external connections.



VLSI Master, “Introduction to FPGA & CPLD

What is Inside an FPGA?

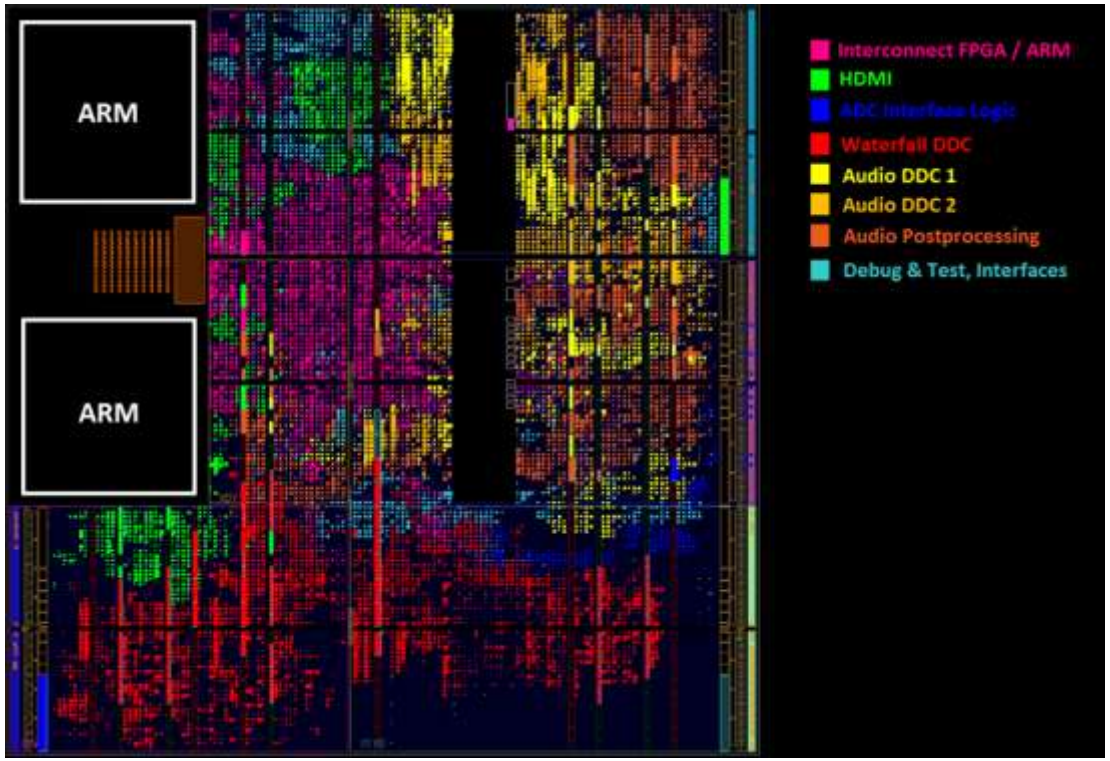
- What is a CLB?
  - A Configurable Logic Block (CLB) is a programmable circuit inside an FPGA.
  - Think of it like LEGO bricks for digital circuits—each CLB can be configured for different tasks.
- What's Inside a CLB?
  - Look-Up Tables (LUTs): Store logic functions.
  - Flip-Flops (FFs): Hold values for sequential operations.
  - Carry Chains: Optimize arithmetic operations.
  - Multiplexers (MUX): Decide which signals to use.
- Why is CLB Hardware Important in Design?
  - Every logic operation, memory storage, and computation needs CLB resources.
  - More features = More CLBs = Higher FPGA cost & power consumption.



Petter.kallstrom, Public domain, via Wikimedia Commons

Why Mathematical Derivation Is Needed for an FPGA

- FPGA hardware cannot simply call high-level mathematical functions.
- The computation must use a fixed, deterministic sequence of basic operations.
- Matrix operations and iterative algorithms must be rewritten into hardware-ready steps.
- Fixed-point arithmetic requires explicit choices about scaling and numerical precision.
- Common software tools do not directly map to FPGA hardware:
  - built-in ellipse-fitting functions,
  - unbounded while loops, and
  - double-precision floating-point arithmetic.



Panoradio SDR: Advanced Software Defined Radio

Current Work

FPGA-friendly ellipse fitting derivation

Every point in the embedded cloud contributes one row to D. The scatter matrix collects the sums required for ellipse fitting.

The coefficients minimize the algebraic distance while the Fitzgibbon constraint guarantees an ellipse.

Partitioning the system eliminates the linear coefficients before solving the smaller quadratic problem.

The reduced 3 by 3 system gives the quadratic coefficients that control ellipse shape and orientation.

Back-substitution computes the coefficients from a_1. Normalization fixes the arbitrary eigenvector scale.

Design and scatter matrices

$$d_k = [x_k^2, x_k y_k, y_n^2, x_k, y_k, 1]$$
$$D = [D_1 \mid D_2]$$
$$D_1 = [x^2, xy, y^2]$$
$$D_2 = [x, y, 1]$$
$$S = D^T D = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix}$$
$$a_1 = [a, b, c]^T, \quad a_2 = [d, e, f]^T$$

Constrained ellipse fit

$$F(x, y) = ax^2 + bxy + cy^2 + dx + ey + f = 0$$
$$\min \; a^T S a$$
$$\text{subject to} \; a^T C a = 1$$
$$4ac - b^2 = 1$$
$$L(a, \lambda) = a^T S a - \lambda(a^T C a - 1)$$
$$S a = \lambda C a$$

Schur-complement reduction

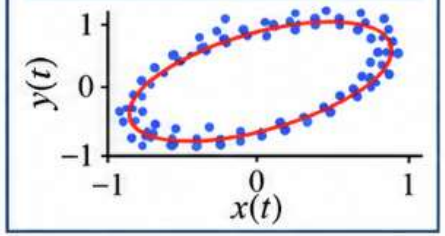
$$S_{11} a_1 + S_{12} a_2 = \lambda C_1 a_1$$
$$S_{21} a_1 + S_{22} a_2 = 0$$
$$a_2 = -S_{22}^{-1} S_{21} a_1$$
$$S^* = S_{11} - S_{12} S_{22}^{-1} S_{21}$$
$$S^* a_1 = \lambda C_1 a_1$$
$$6 \text{ x } 6 \text{ to } 3 \text{ x } 3$$

Eigenvalue solution

$$A = C_1^{-1} S^*$$
$$A a_1 = \lambda a_1$$
$$\{(\lambda_1, v_1), (\lambda_2, v_2), (\lambda_3, v_3)\}$$
$$a_1 = v_{k^*}, \quad k^* = \arg\min |\lambda_k|$$
$$\text{require } b^2 - 4ac < 0$$

Recover and normalize coefficients

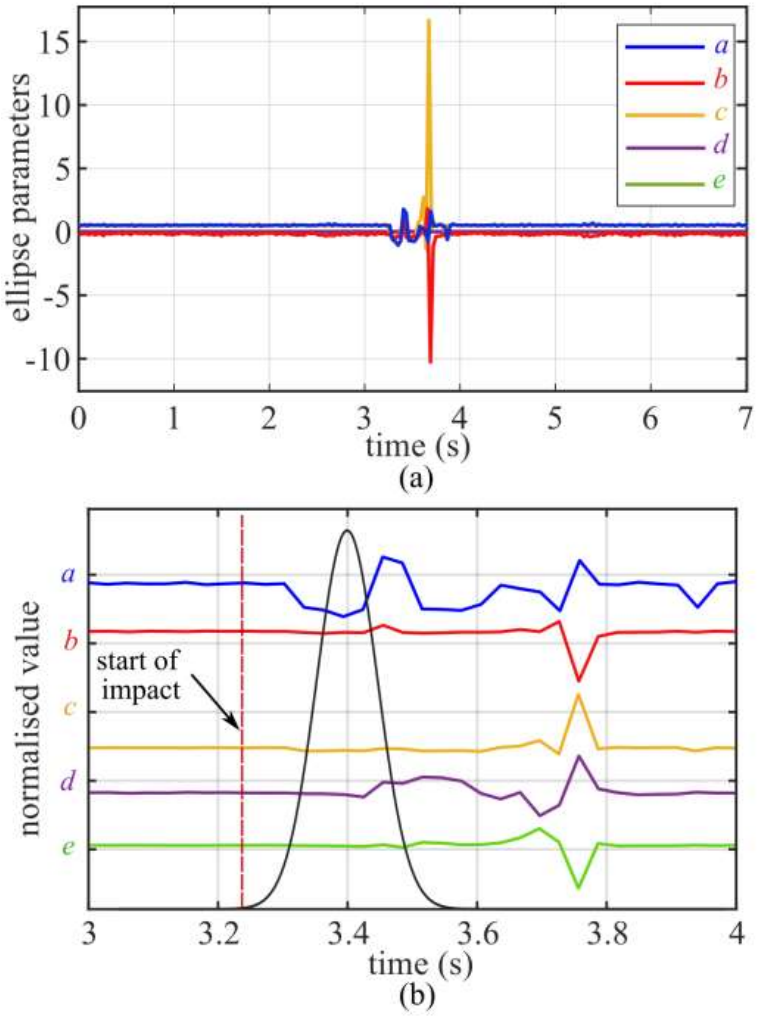
$$a_2 = -S_{22}^{-1} S_{21} a_1 = [d, e, f]^T$$
$$a = [a_1; a_2] = [a, b, c, d, e, f]^T$$
$$\sigma = \sqrt{|4ac - b^2|}$$
$$a_{\text{norm}} = a / \sigma$$
$$a_{\text{norm}}^T C a_{\text{norm}} = 1$$



Ellipse Parameters Reveal Shock incident

- Ellipse coefficients remain nearly stable during harmonic vibration.
- The shock causes sharp excursions in the coefficients.
- Parameter *a* gives the fastest response for the presented experiment.

$$F(x, y) = ax^2 + bxy + cy^2 + dx + ey + f = 0$$



Ellipse parameters coefficient and shock incident

Conclusion

- Fast-TDA detects shock-induced changes in PCB acceleration responses through the geometry of delay-embedded point clouds.
- Direct ellipse fitting replaces repeated persistence-diagram computation required by conventional TDA.
- A sequential change-point detector could use the Fast-TDA feature stream to localize shock onset with minimal delay.

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Discussion

Paper 2026 FPGA-deployable Approximate Topological Framework

https://github.com/ARTS-Laboratory/Paper-2026-FPGA-Deployable-Approximate-Topological-Framework

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