ADAPTIVE SHOCK TESTING AND FAILURE PREDICTION OF PRINTED CIRCUIT BOARDS USING KRIGING-BASED EXPERIMENTAL DESIGN

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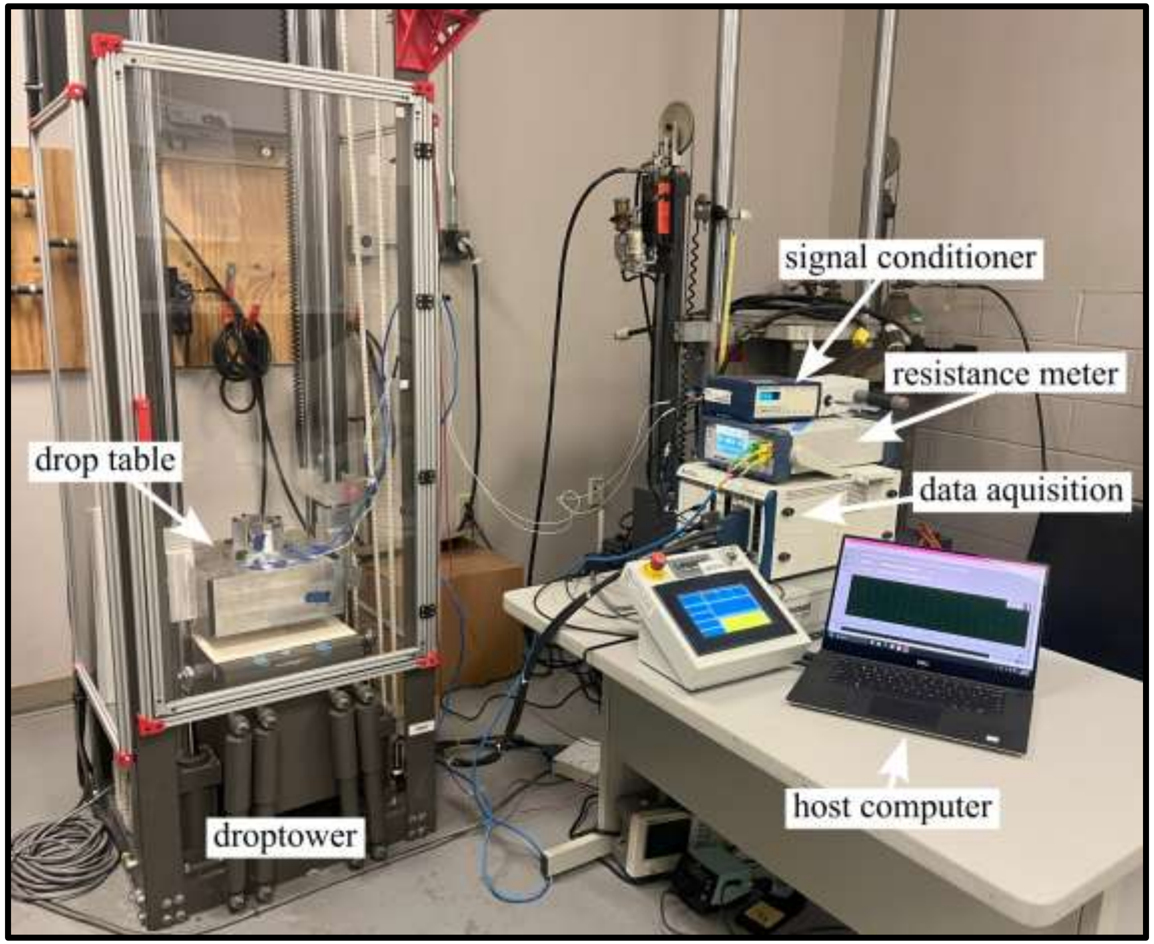
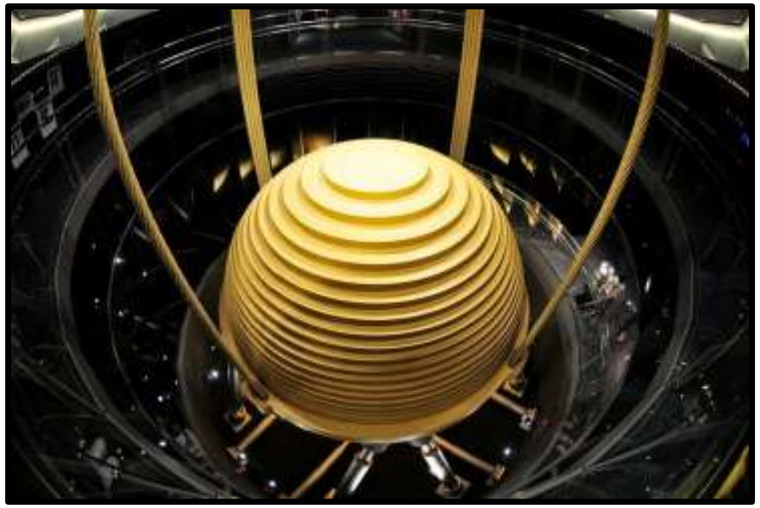
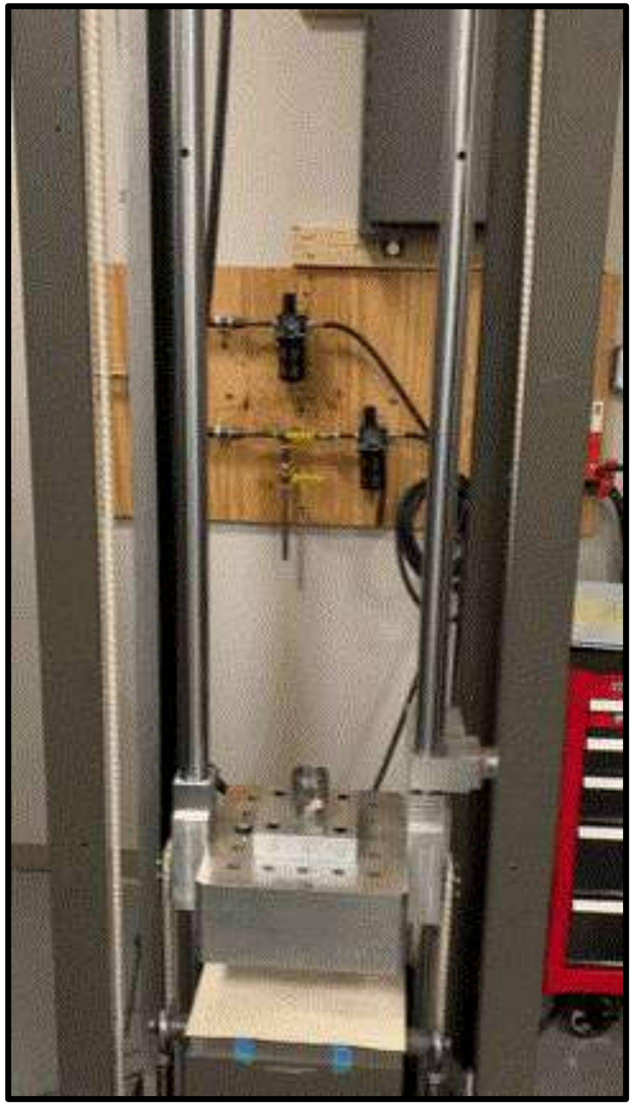


INTRODUCTION

WHAT IS SHOCK?

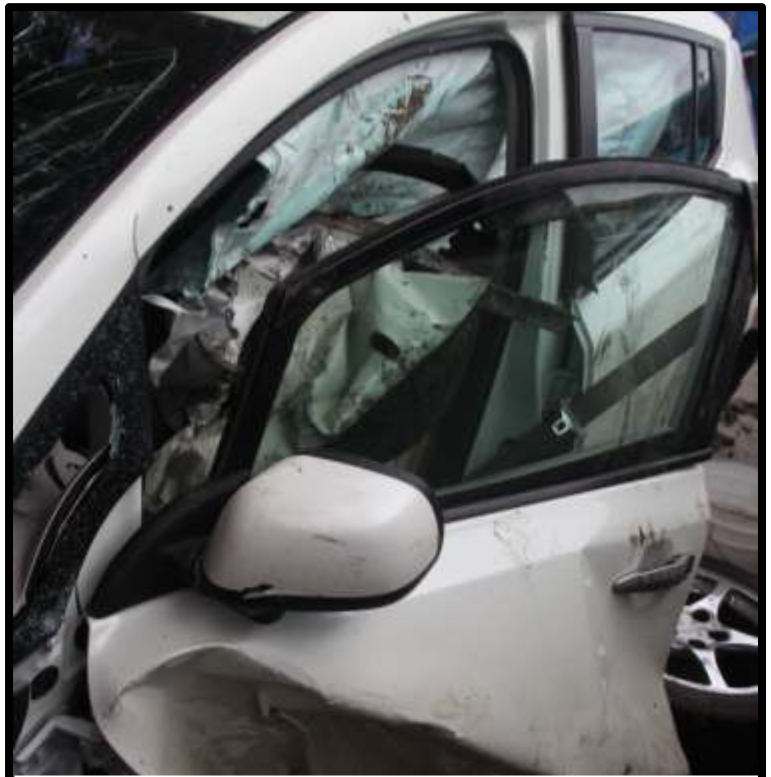
- Sudden, high-amplitude acceleration impulse (μs–ms duration)
- Broadband excitation with significant high-frequency content
- Generates extreme stress gradients and localized damage mechanisms
- Highly non-stationary and sensitive to boundary conditions
- Difficult to model and predict





REAL-WORLD APPLICATIONS

Blast Against Civil Structures



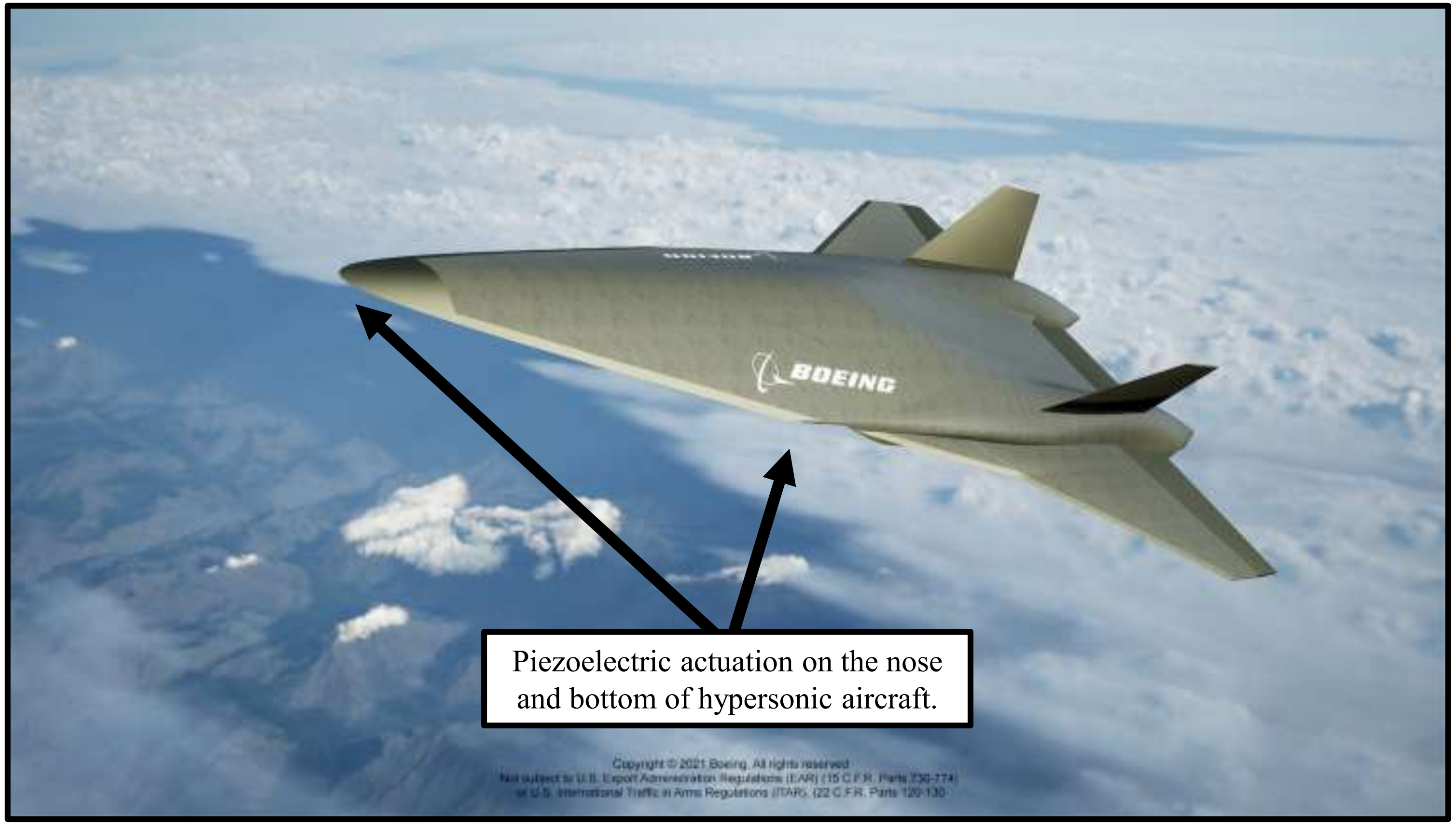
Automotive Impact and Crashes

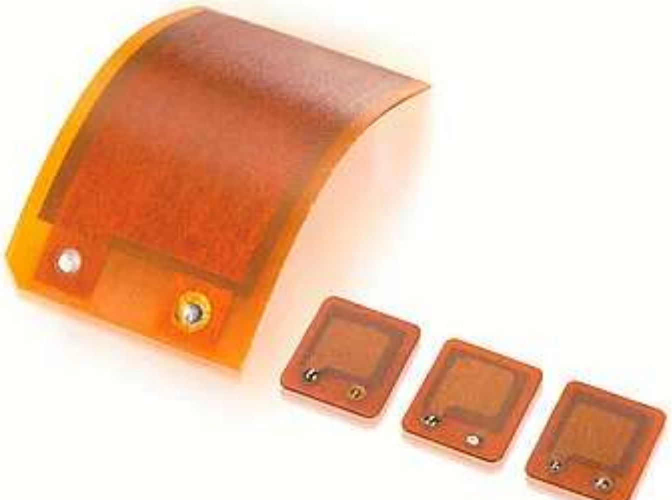
High-speed Aircraft and Airframes

MOTIVATION

- PCBs are the structural and electrical backbone of nearly all modern electronic systems
- Repeated shock causes progressive damage like solder joint fatigue, trace delamination, and interconnect fracture, often silently before catastrophic failure
- Understanding how shock response correlates with physical degradation is critical for predicting failure and designing more resilient hardware

PROJECT GOAL



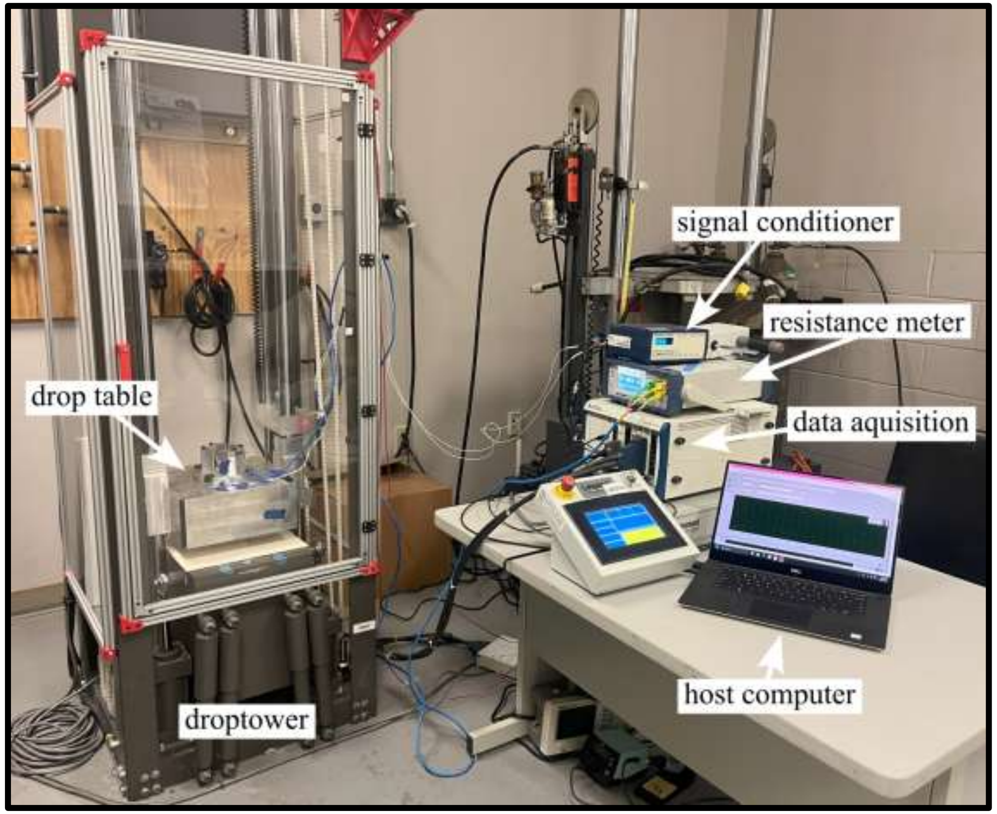


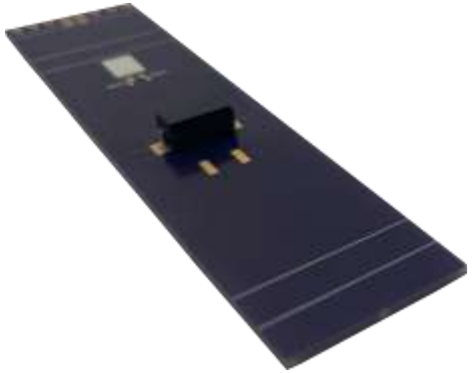
PZT Actuator Patches

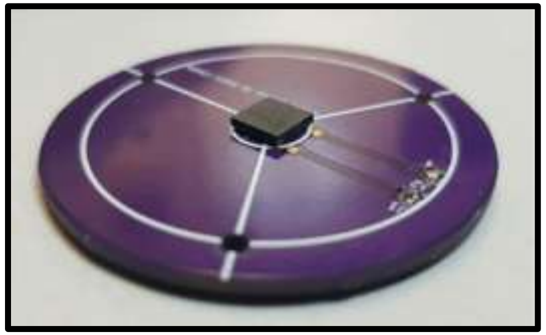
ONGOING WORK

EXPERIMENTAL PLATFORMS

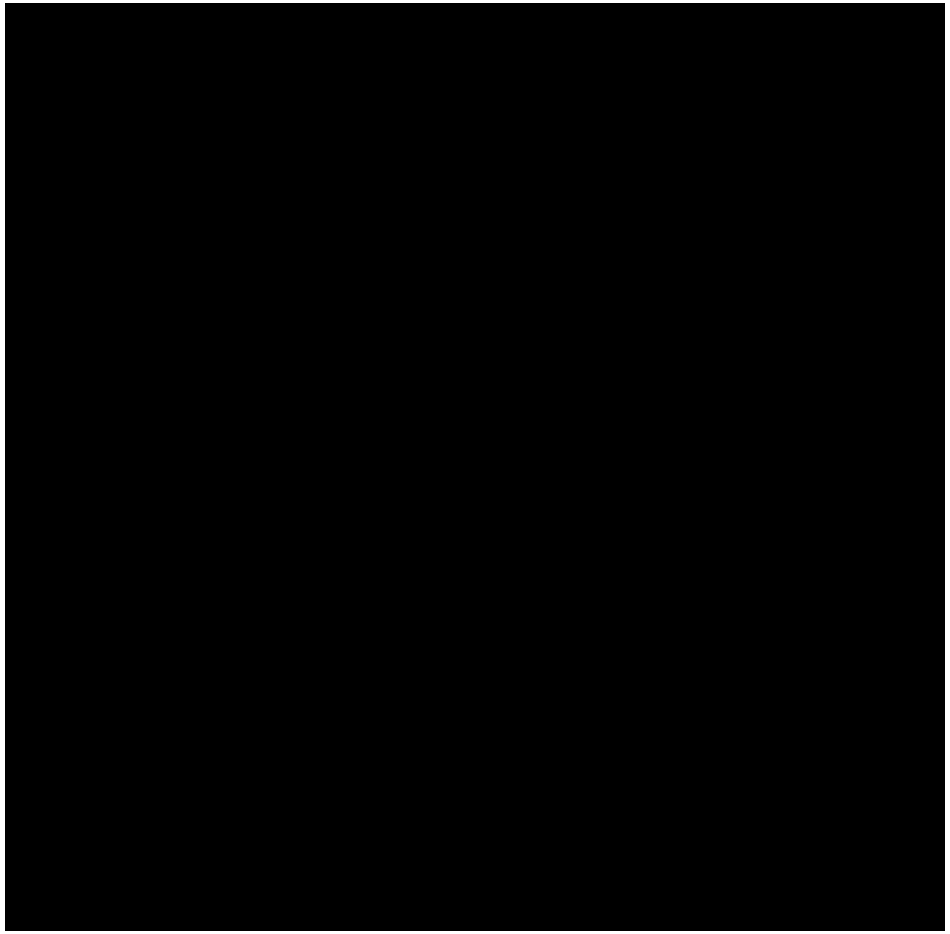
- Shock testing across multiple PCB geometries (circular, cantilever, fixed–fixed)
- Component-level fatigue studies (resistors, BGA dummy components)
- Controlled variation of impact energy and boundary conditions
- Creation of labeled, high-rate degradation datasets

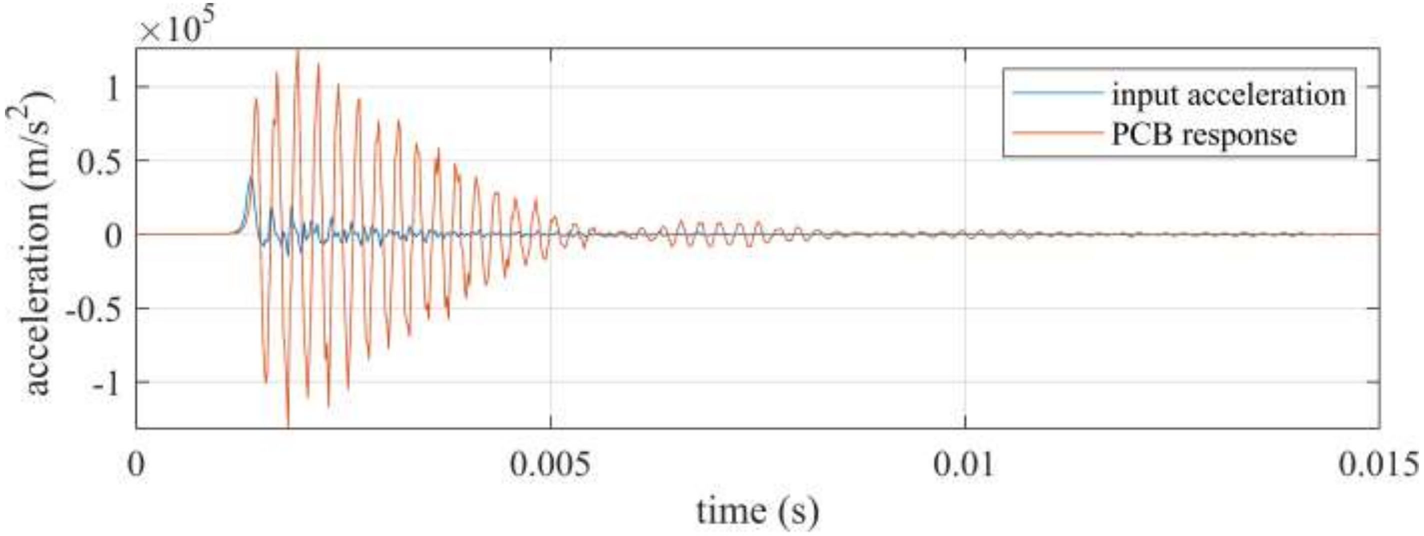


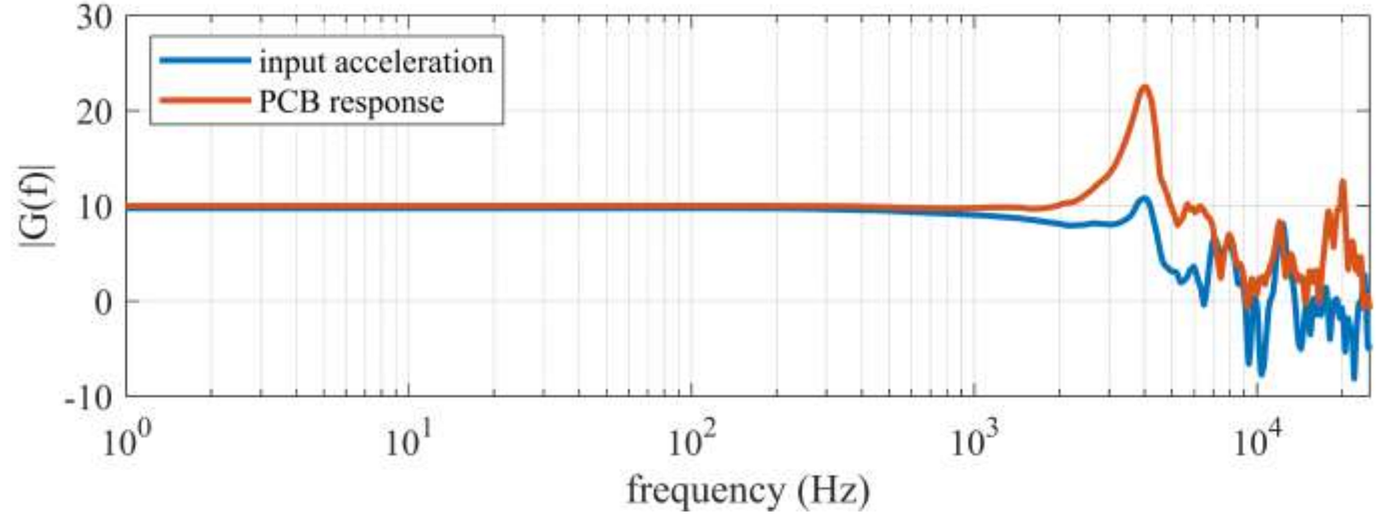




DATASET COLLECTION

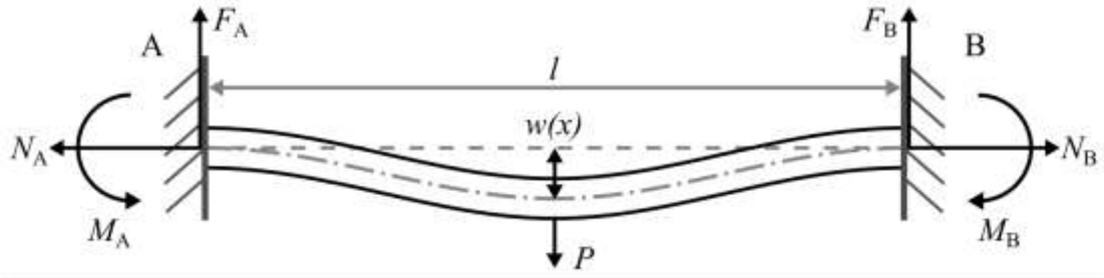


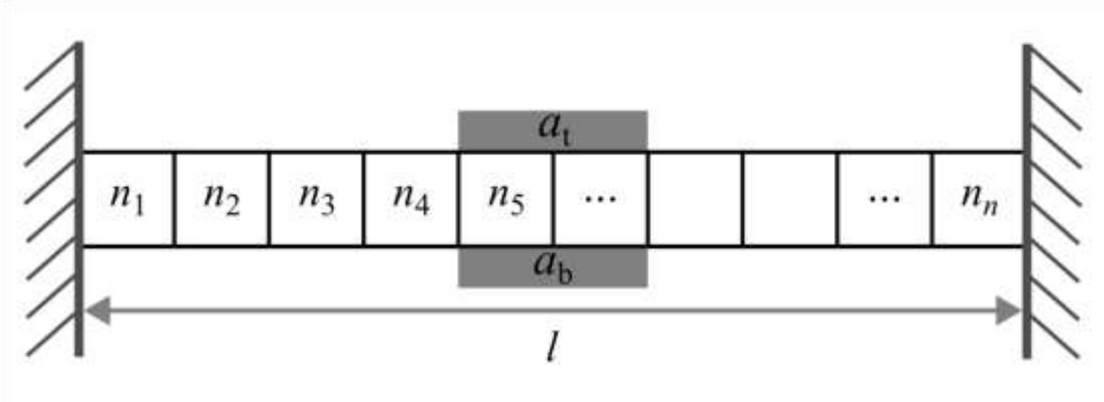


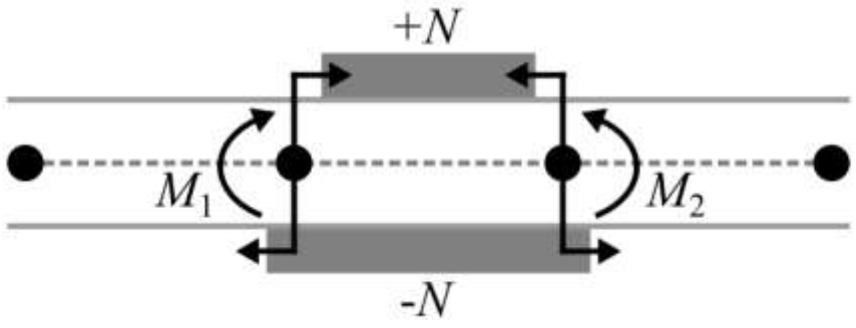


REDUCED-ORDER MODELING OF SHOCKED PCBS

- Extended Euler–Bernoulli beam with axial–bending coupling
- Moment-based actuation to emulate piezo patches
- Validated against higher-fidelity shell model
- Captures dominant bending dynamics under ~5000 g transient loads







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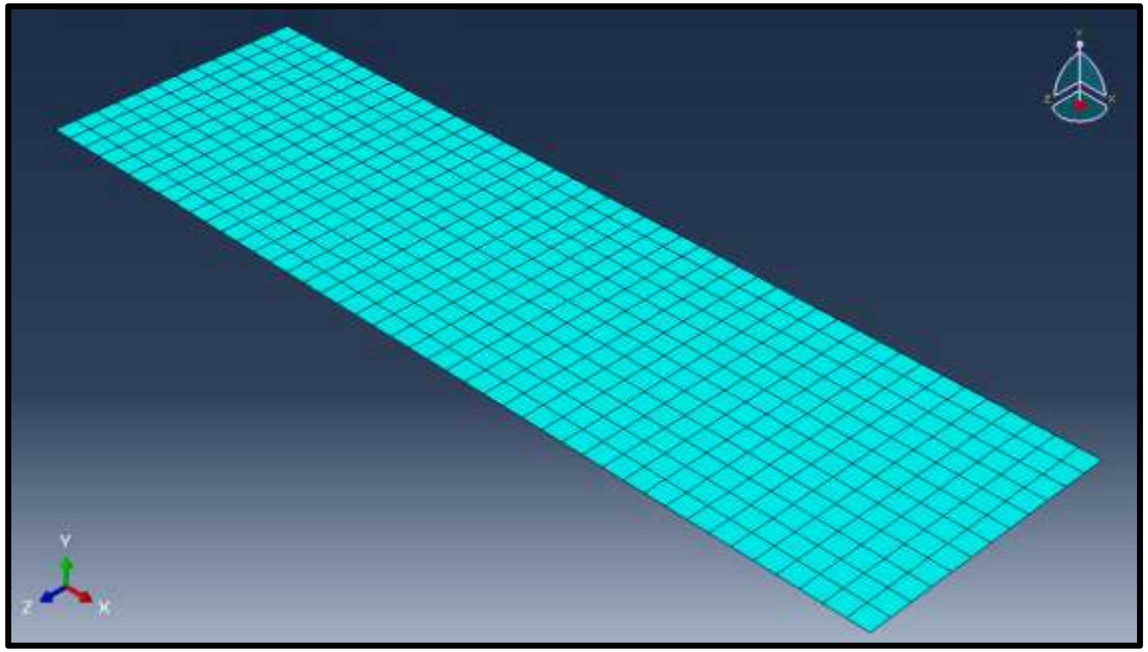
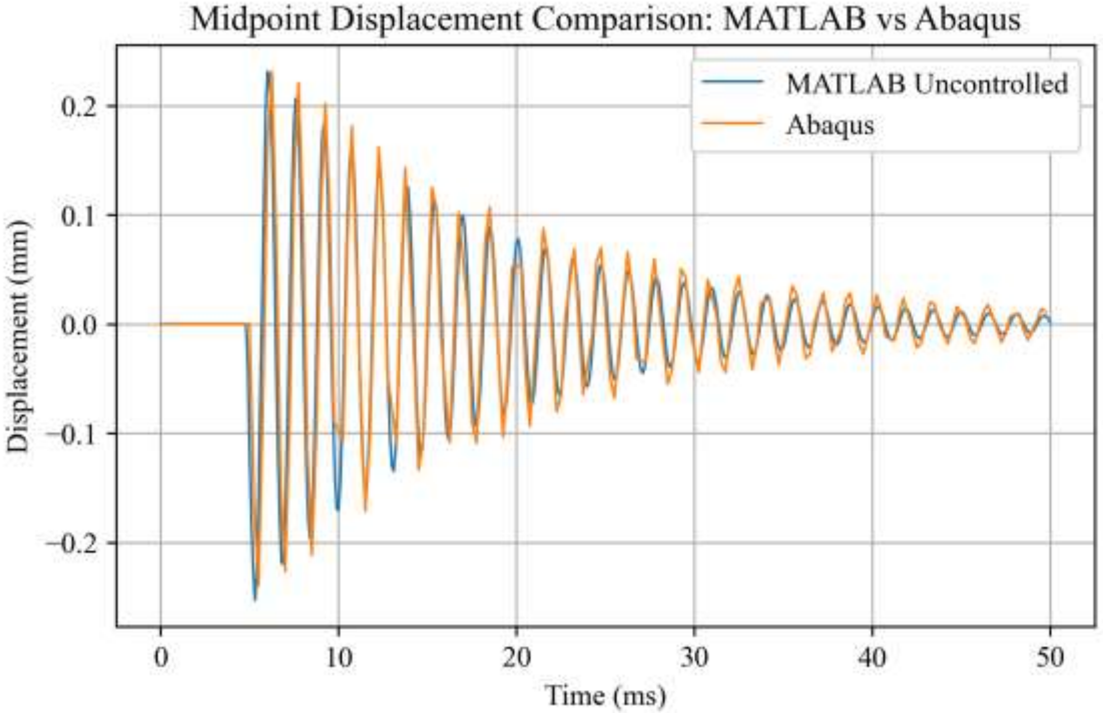
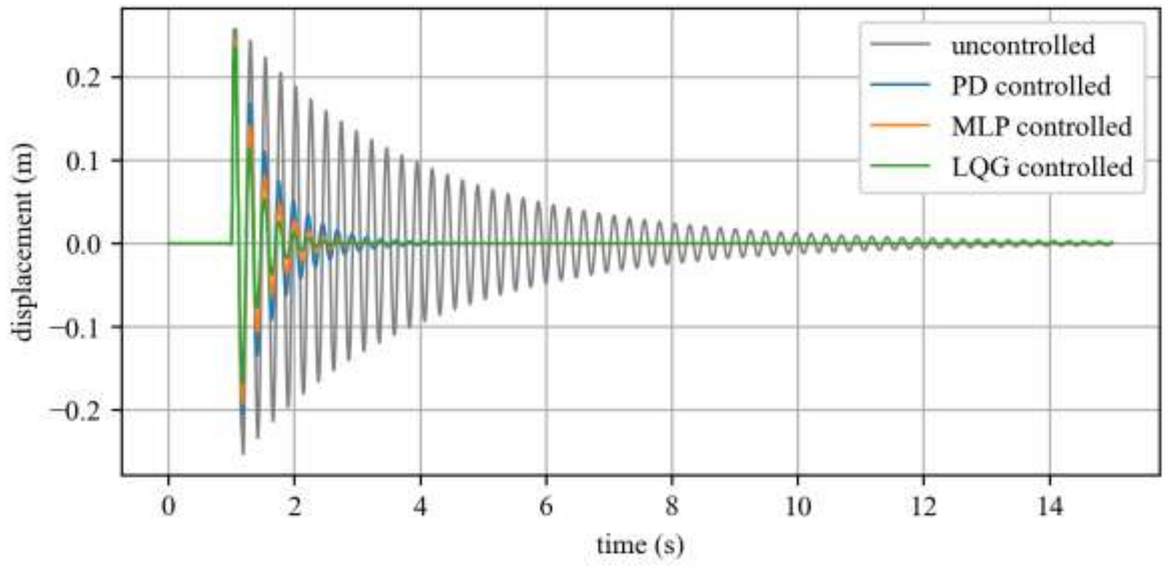
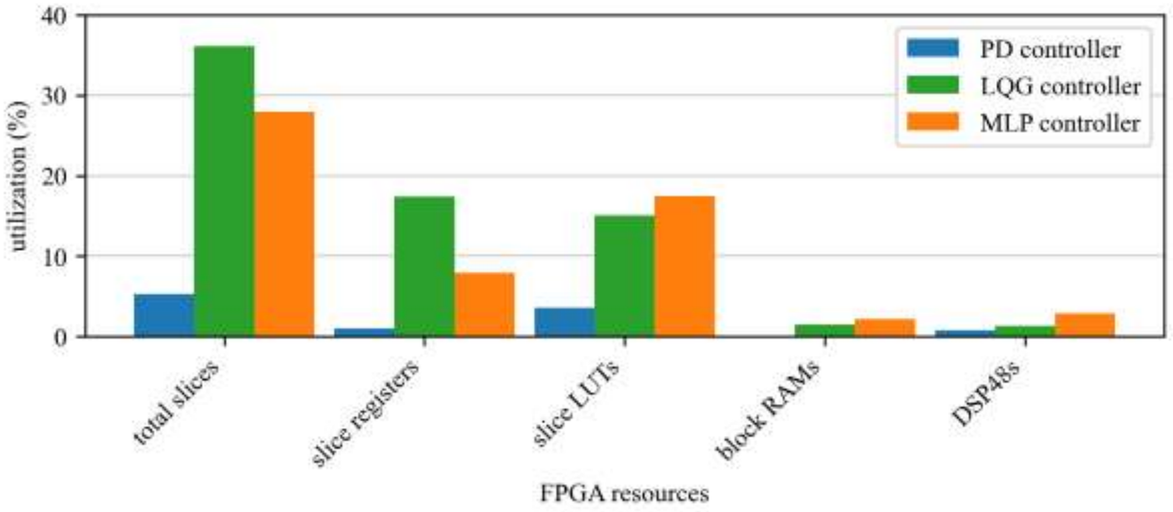




LOW-LATENCY CONTROL DEPLOYMENT

- FPGA implementation of PD, LQG, and MLP controllers
- Resource and performance benchmarking
- Learning-based control reduces hardware cost
- Sub-millisecond execution potential

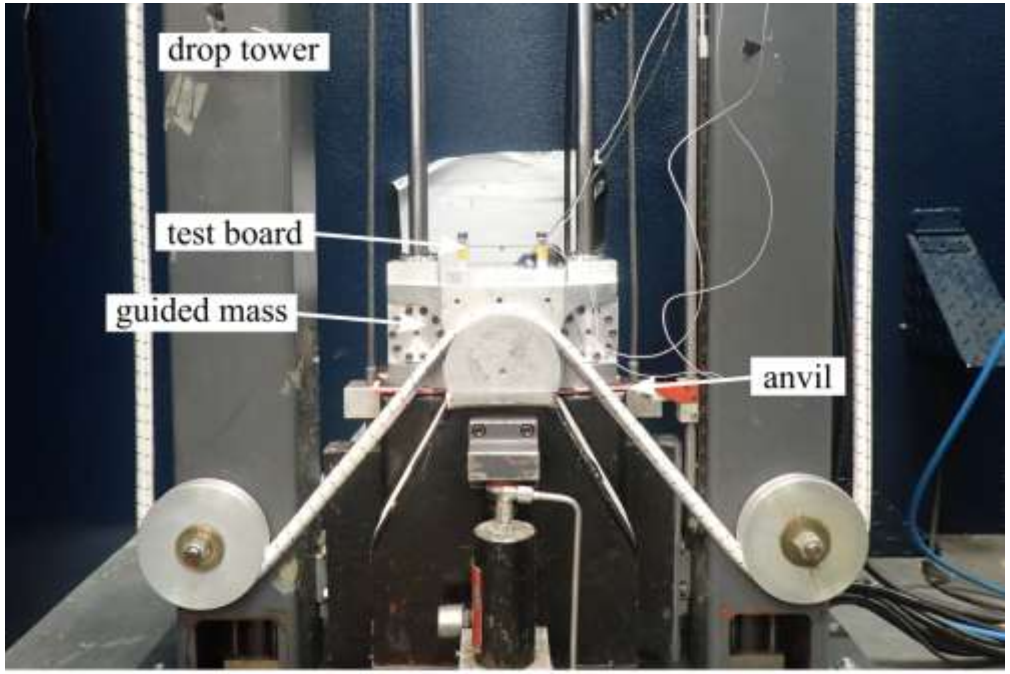


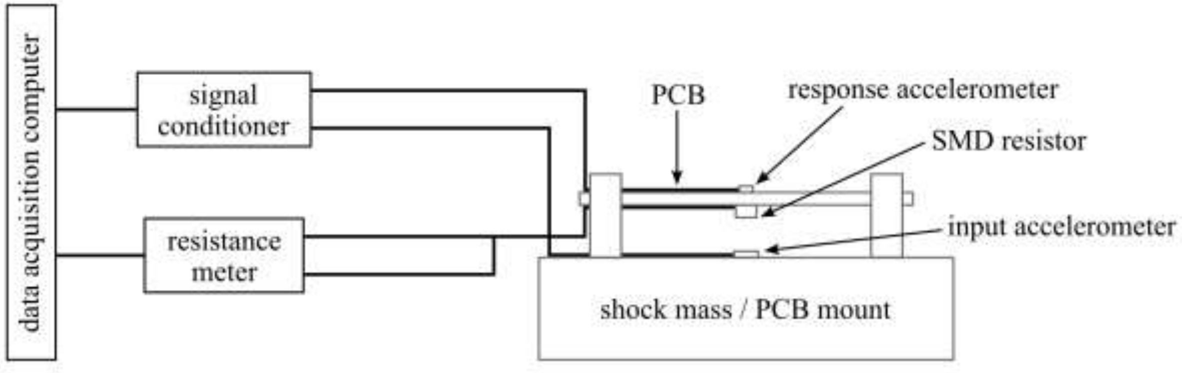


FOCUSED STUDY

EXPERIMENTAL DESIGN

- 75 Tg FR4 PCB: 25.4 × 88.9 × 1.6 mm, fixed-fixed beam boundary conditions
- Single 1 kΩ SMD resistor at midspan; failure defined as open-circuit
- Acceleration range: 5,000 – 12,000 g; pulse duration: 0.13 – 0.33 ms
- Signals sampled at 2 MHz; lifetimes recorded from 1 to 65 drops



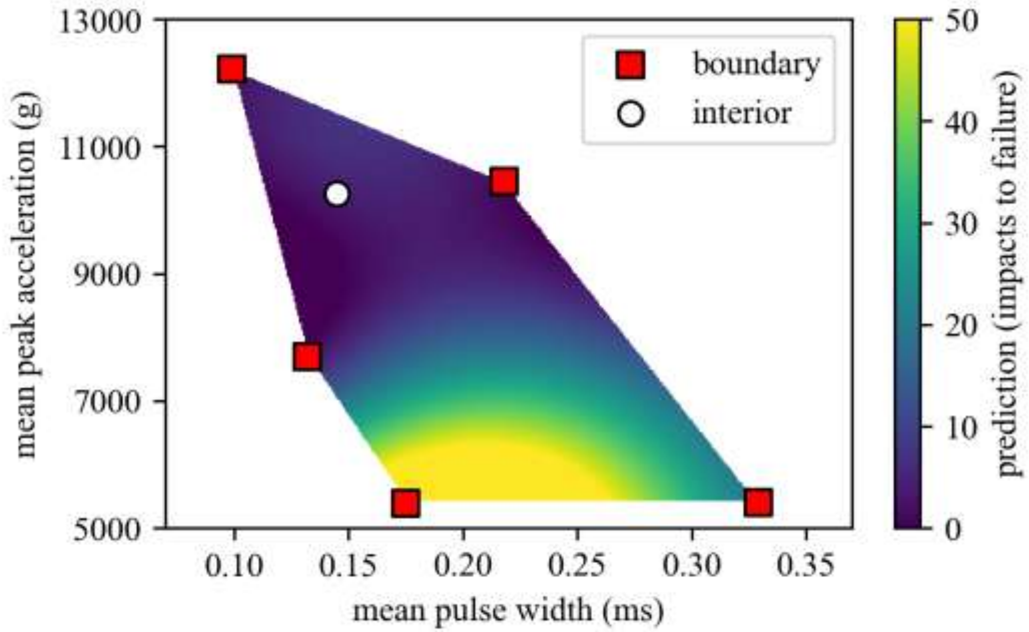


KRIGING SURROGATE MODEL

- Input vector: peak acceleration a and pulse duration τ; output: predicted impacts-to-failure
- Universal Kriging decomposes response as

$$y(x) = m(x) + \varepsilon(x)$$

- Gaussian variogram fit over the 2D acceleration–duration domain
- Evaluated on a fixed Cartesian grid to produce continuous prediction field P(x)

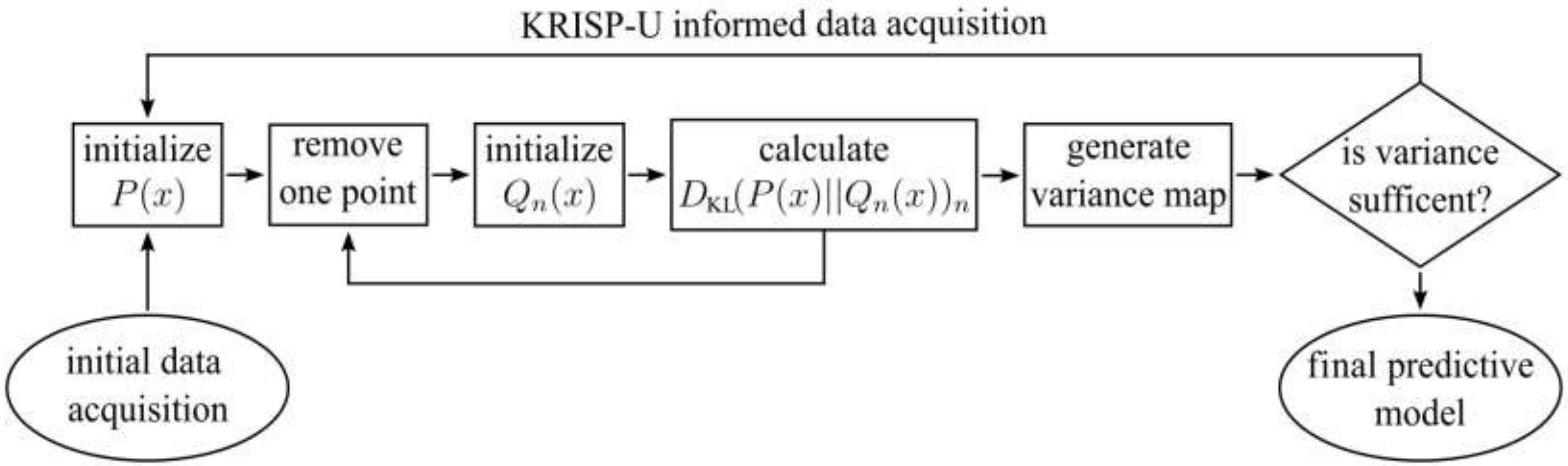


KRISP-U ADAPTIVE SAMPLING

- Leave-one-out cross-validation repeated for each interior data point
- KLD score per point; larger v_n = higher local uncertainty

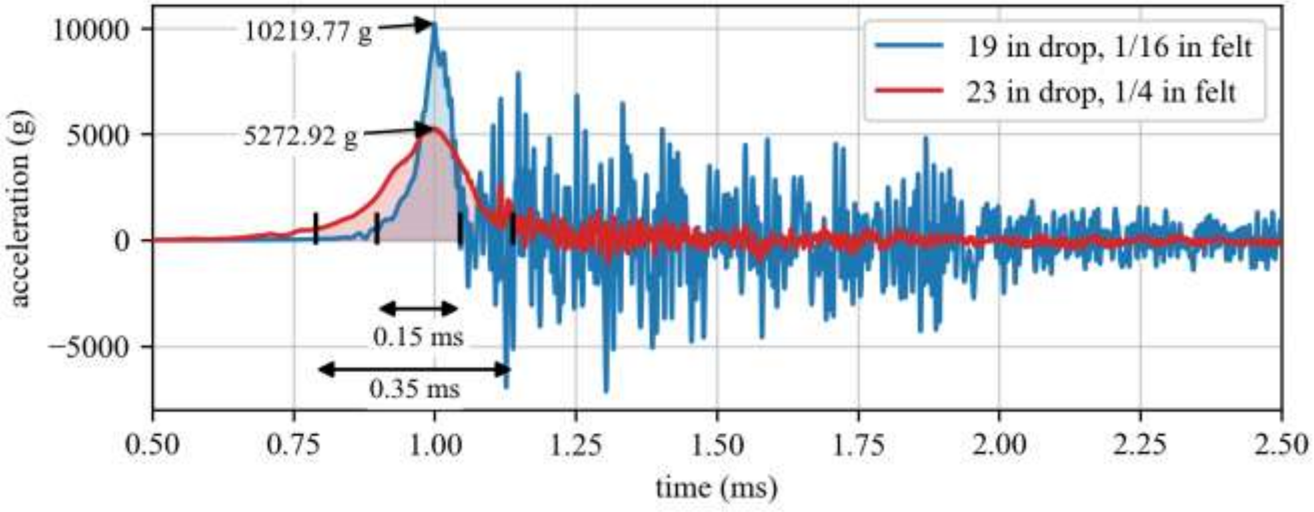
$$v_n = D_{KL}(P(x) \parallel Q_n(x))$$

- Continuous variance map interpolated from scores; next test placed at argmax v(x)
- Boundary points fixed; only interior points contribute to variance scoring



DATASET OVERVIEW

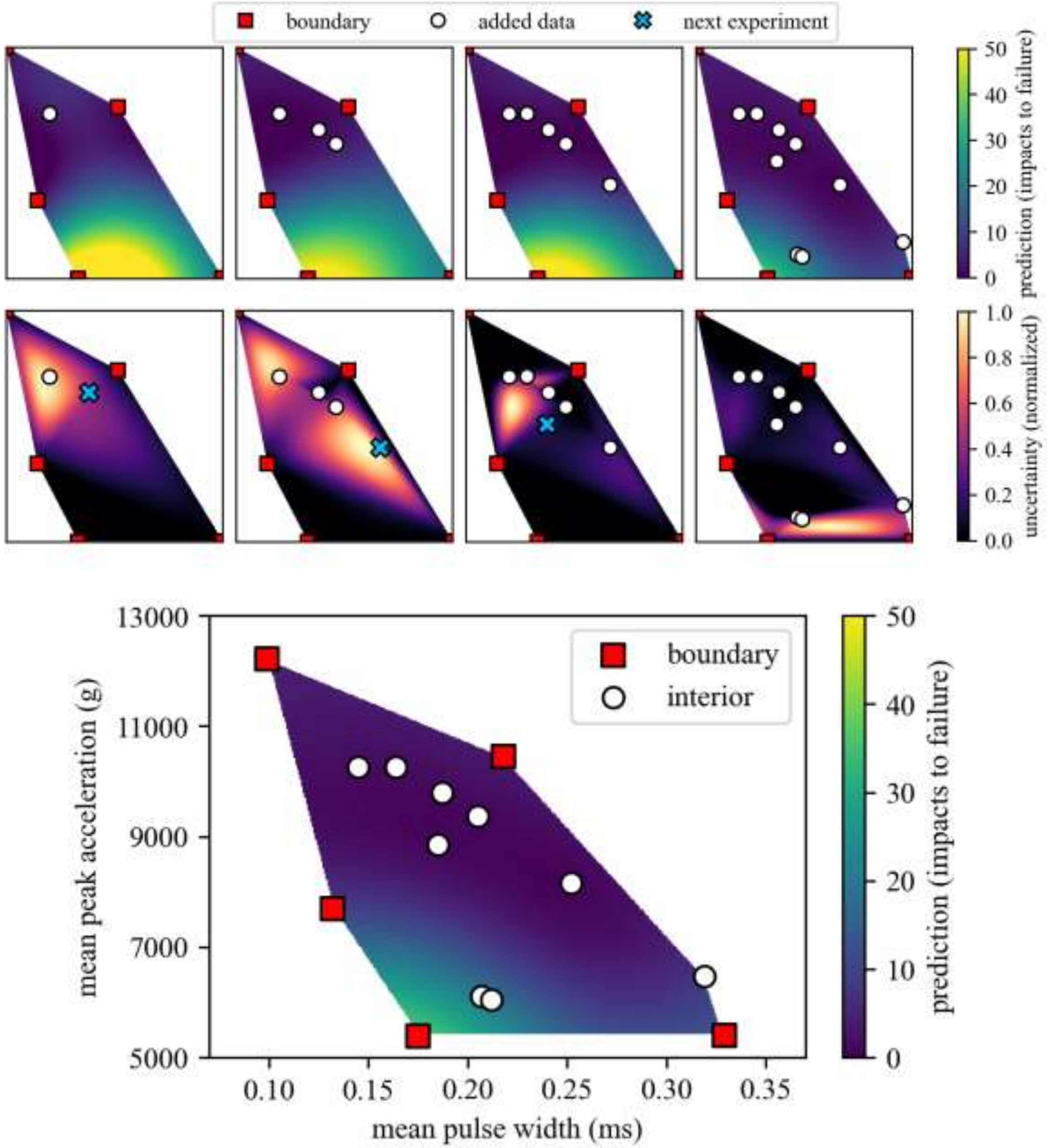
- 14 tests total: 5 boundary, 6 operator-selected, 3 KRISP-U algorithmic
- Acceleration: 5,387 – 12,211 kg_n; pulse width: 0.099 – 0.329 ms
- Impacts to failure: 1 up to 65 at lowest acceleration condition
- Similar acceleration levels produced 1–13 impacts depending on pulse duration



data set	mean pulse width (ms)	mean peak acceleration (kg_n)	ΔV (km/s)	impacts to failure	class
1	0.175	5.387	5.888	65	boundary
2	0.099	12.211	7.550	2	boundary
3	0.329	5.401	13.222	19	boundary
4	0.218	10.446	14.222	1	boundary
5	0.132	7.691	6.340	2	boundary
6	0.145	10.254	9.286	4	operator
7	0.187	9.788	11.431	1	operator
8	0.205	9.364	11.988	1	operator
9	0.252	8.162	12.845	3	operator
10	0.164	10.260	10.508	1	algorithmic
11	0.185	8.858	10.234	3	algorithmic
12	0.207	6.111	7.900	13	operator
13	0.319	6.469	12.888	3	operator
14	0.212	6.045	8.004	6	algorithmic

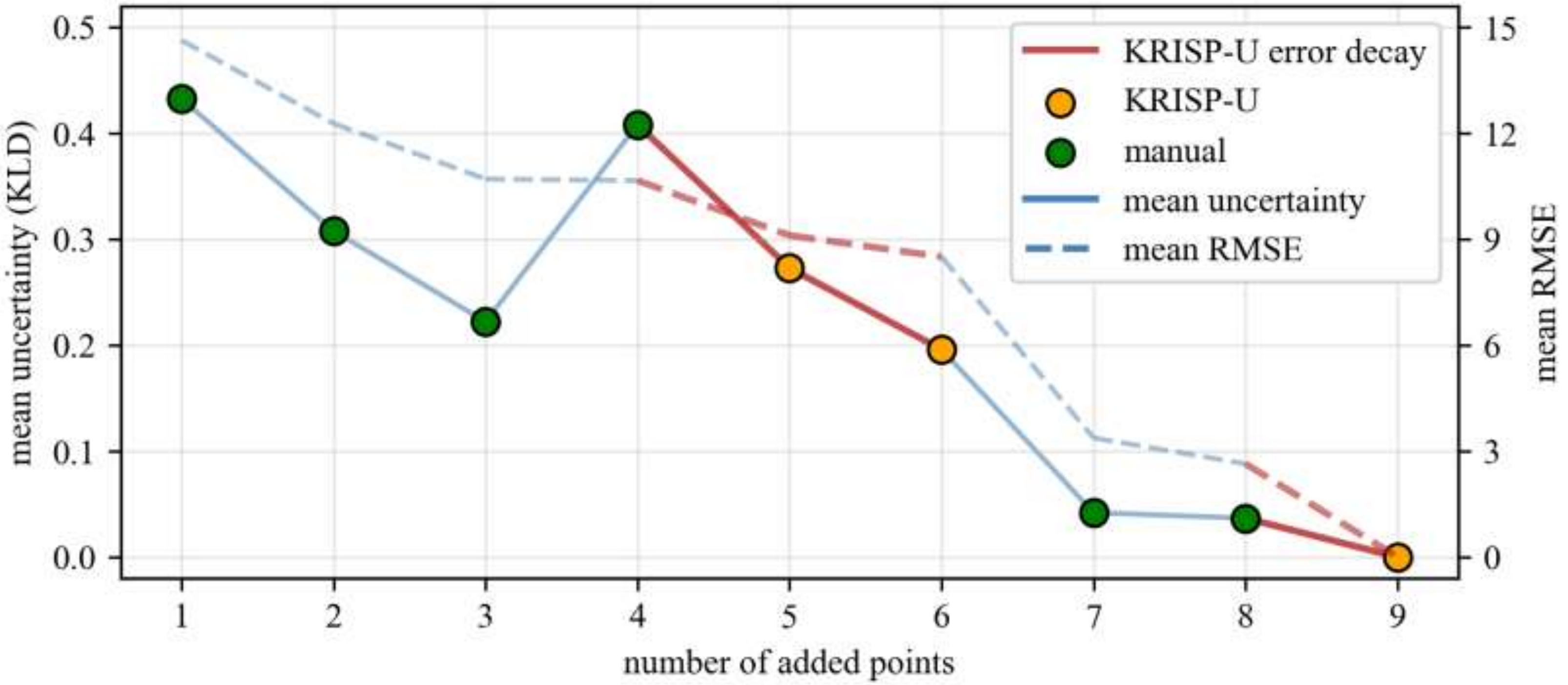
RESULTS

- Surrogate initialized on 5 boundary points; 9 interior points added iteratively
- KRISP-U points: more consistent KLD and RMSE reduction than manually selected points
- Final RMSE near 0; mean KLD converged to ~0 by iteration 9
- Survivability drops sharply above ~9,000 g across all tested pulse durations



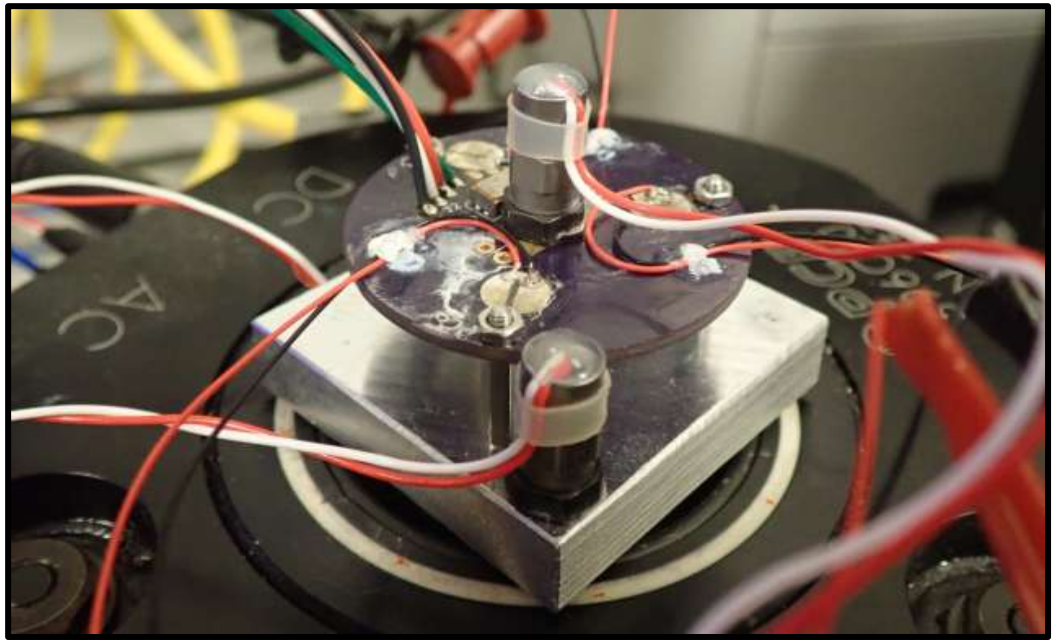
CONCLUSION

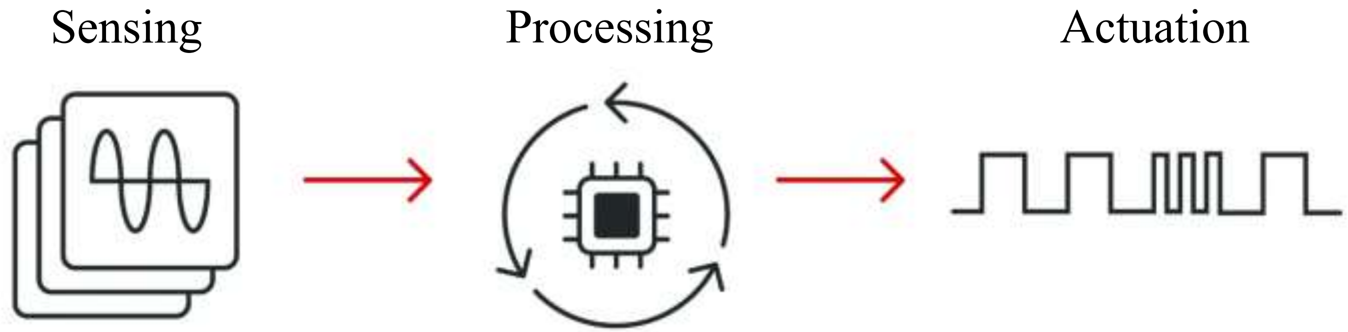
- 14 tests sufficient to map PCB failure across 5,000–12,000 g and 0.13–0.33 ms
- KRISP-U reduced mean uncertainty from ~0.45 KLD to ~0.01 over 9 iterations
- Framework applicable to other geometries, components, and loading conditions



RESEARCH TRAJECTORY

- Develop low-latency degradation state estimators deployable on embedded hardware (FPGA)
- Integrate cumulative damage indicators into adaptive control frameworks
- Extend modeling from simplified beam systems to component-level PCB assemblies
- Investigate physics-informed learning for degradation-aware control
- Piezoelectric sensing/actuation experimentation.





QUESTIONS?

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