Power Characterization of Edge-Based FFT Processing in a SWaP-Constrained Wearable Platform

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Introduction

- Edge computing enables real-time signal processing in SWaP-constrained embedded systems but increases power consumption and reduces battery life. Understanding these energy trade-offs is critical for designing efficient wearable devices.
- This work compares the power consumption of onboard FFT processing with conventional raw data logging using a custom PPG heart rate monitor.

Methods

- PATCH heart rate tracker integrated onto a custom HDK for power measurement and thermal imaging.
- Powered using a National Instruments PXIe Power Source Measurement Unit configured as 3.7V 600 mAh LiPO battery emulator.
- Offline FFT algorithm adapted for real-time execution within embedded memory constraints.
- HDK spray painted with matte black paint to reduce reflections.
- Tested in three configurations while capturing thermal imaging:
  - Data Logger
  - Data Logger (No SD)
  - Edge-Based FFT

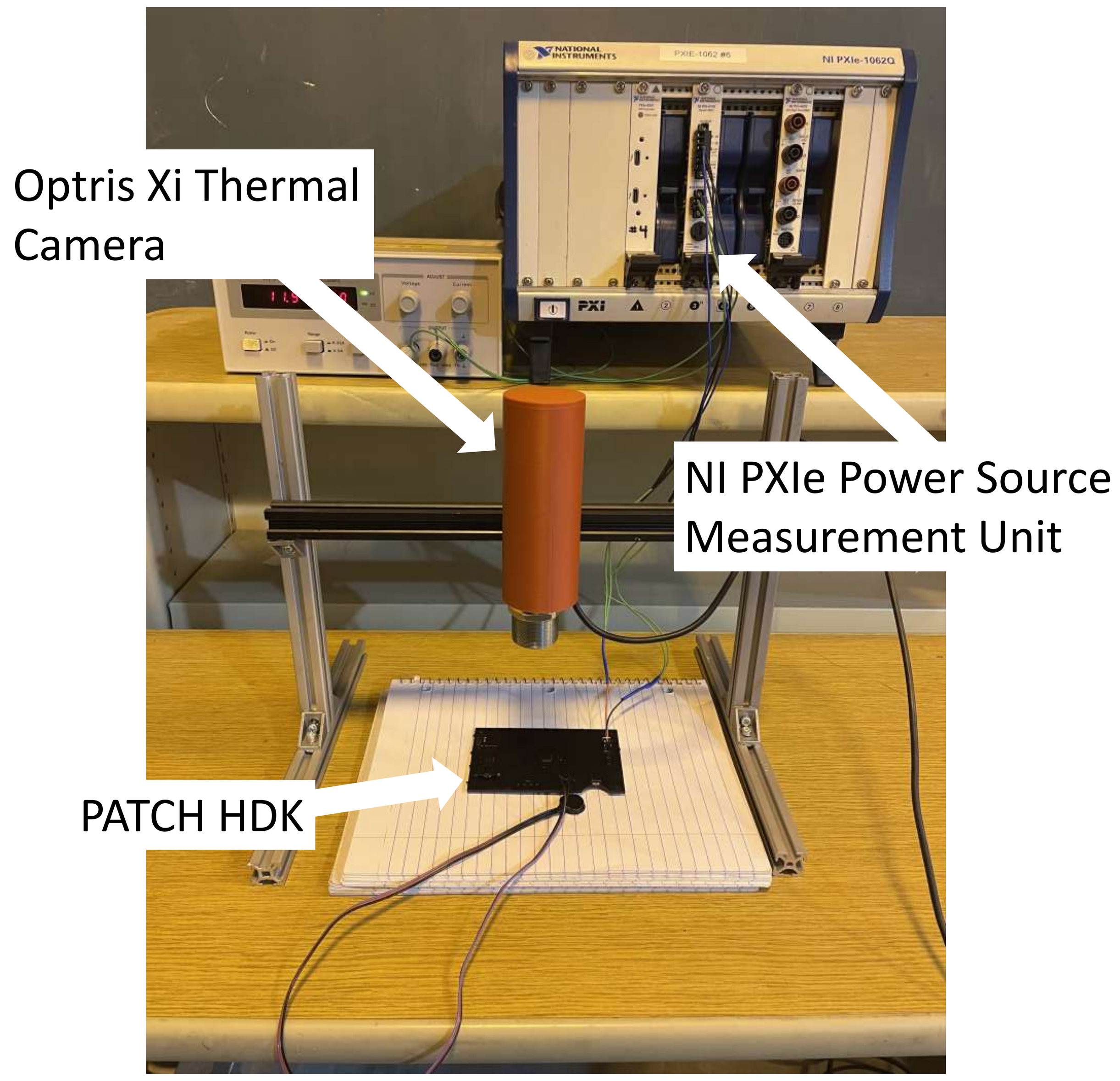

Figure 2. Experimental setup for electrical power characterization and thermal imaging.

Significance

- Understanding the power overhead of edge-based computation enables the development of more energy-efficient SWaP-constrained embedded systems. By quantifying the energy cost of onboard FFT processing relative to data logging, designers can make informed trade-offs between computational performance, battery life, and real-time capability.

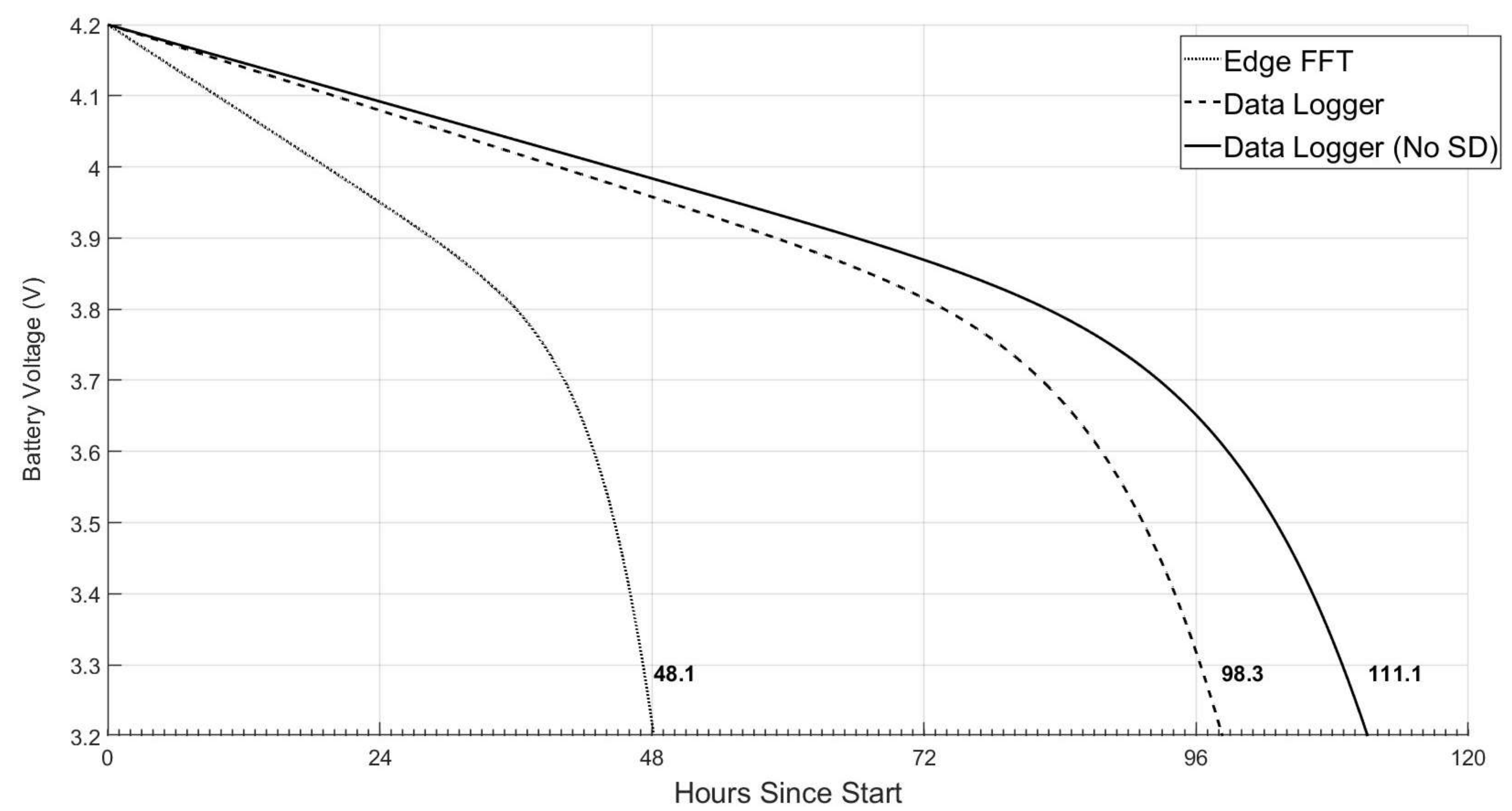

Figure 1. Estimated battery discharge curves generated from measured average current consumption for three embedded processing configurations.

Results

- Edge-based FFT increased average current from 6.13 mA to 11.25 mA (84%) and reduced estimated battery life from 98.3 h to 48.1 h (51%).
- Removing SD card logging reduced average current from 6.13 mA to 5.42 mA (12%) and increased estimated battery life from 98.3 h to 111.1 h (13%).

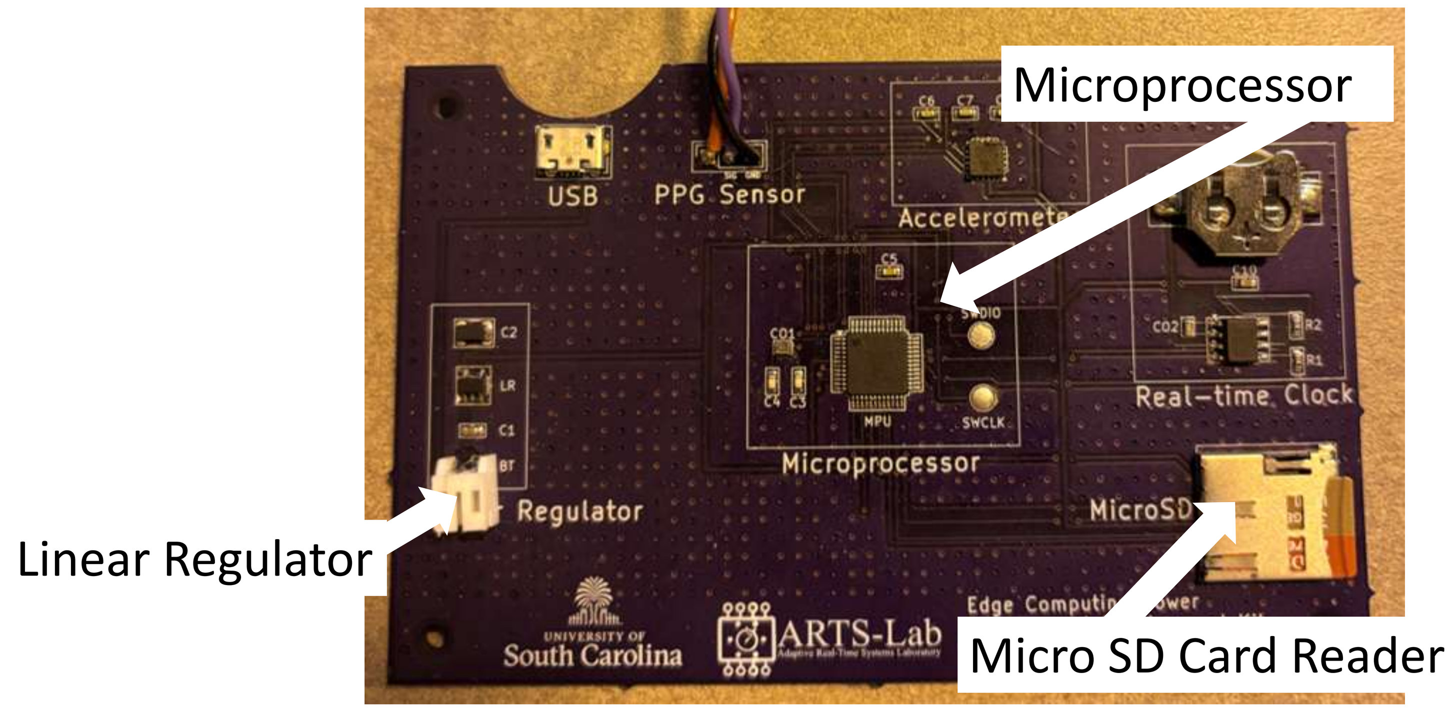

Figure 3. PATCH HDK

Conclusion

- Demonstrated real-time edge-based FFT processing on a SWaP-constrained wearable platform.
- Edge-based processing increased average current consumption by 84%, reducing battery life by 51%.
- Established a quantitative baseline for future embedded power optimization.

Next Steps

- Quantify the computational power overhead of edge-based FFT processing independent of SD card activity.
- Develop an image-processing algorithm to correlate thermal intensity with PXIe power measurements.
- Establish thermal imaging as a quantitative, non-contact tool for embedded power characterization.
- Optimize the embedded FFT implementation to achieve at least a 1.5× increase in battery life while maintaining real-time processing performance.

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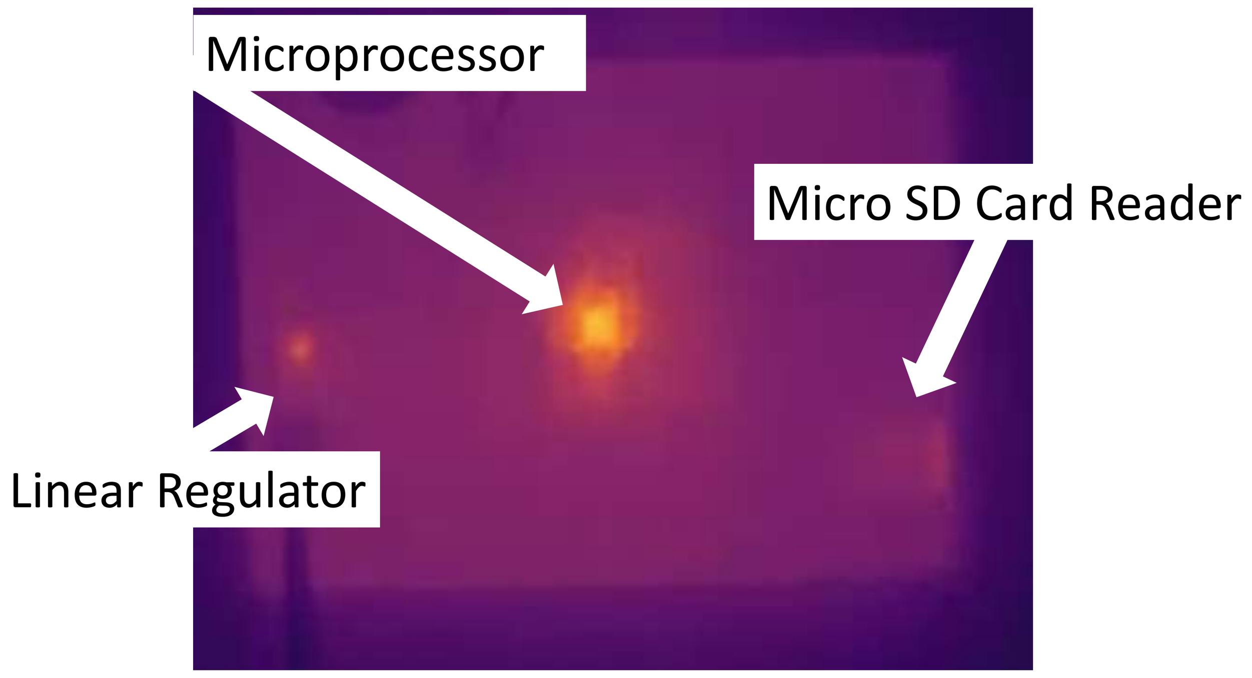

Figure 4. Infrared image of the PATCH HDK showing thermal hotspots.

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