# HARDWARE IMPLEMENTATION OF NONSTATIONARY STRUCTURAL DYNAMICS FORECASTING

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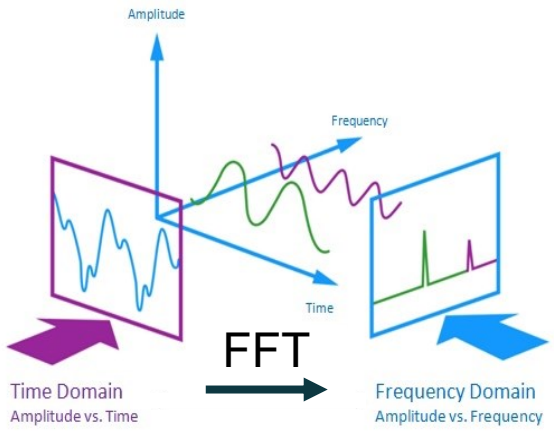
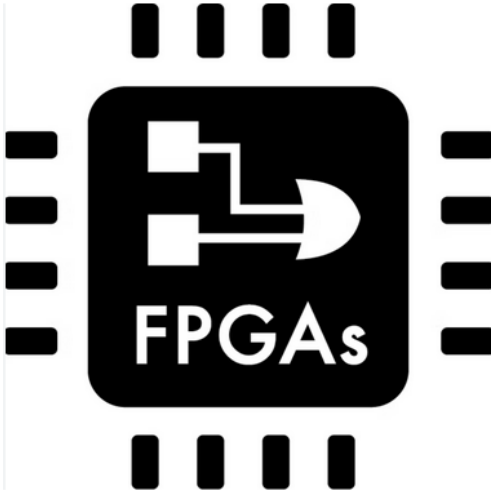
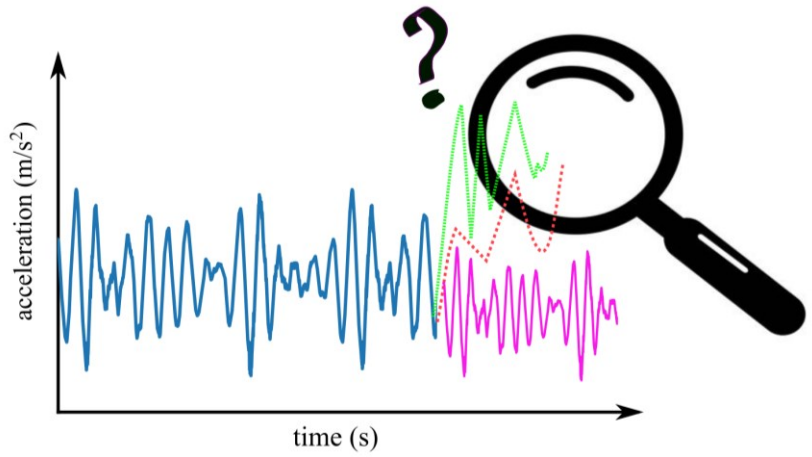


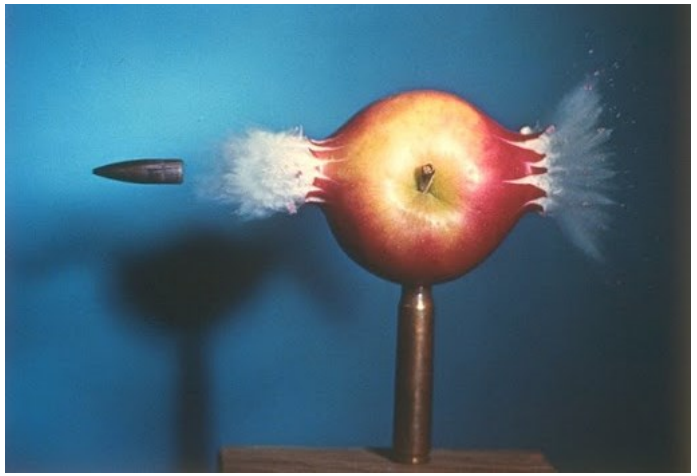



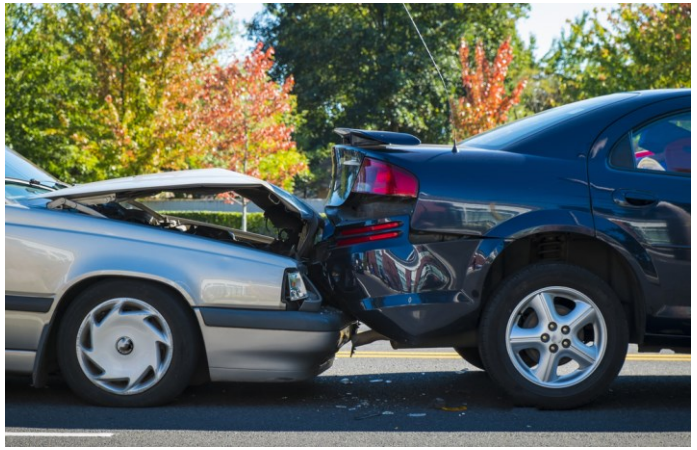



# INTRODUCTION

# HIGH-RATE DYNAMICS

- Description of High-rate dynamics:
  - high-rate (< 100 ms)
  - high-amplitude (acceleration > 100 g)
  - such as a blast or an impact
- The high-rate dynamics are subjected to
  - large uncertainties in external loads
  - high levels of nonstationarities and heavy disturbances
  - generation of unmodeled dynamics from changes in system configuration







Jacob Dodson, Austin Downey, Simon Laflamme, Michael Todd, Adriane G. Moura, Yang Wang, Zhu Mao, Peter Avitabile, and Erik Blasch "High-Rate Structural Health Monitoring and Prognostics: An Overview." Data Science in Engineering, Volume 9, Proceedings of the 39th IMAC, A Conference and Exposition on Structural Dynamics 2021, Springer International Publishing, p. 213-217, Oct 2021. doi:10.1007/978-3-030-76004-5_23

Hong, J., S. Laflamme, J. Dodson, and B. Joyce. 2018. “Introduction to State Estimation of High-Rate System Dynamics,” Sensors, 18(2):217, doi:10.3390/s18010217.

# STRUCTURES WITH HIGH-RATE DYNAMICS

Hypersonic vehicles

Space launch system

Blast seat energy absorbers

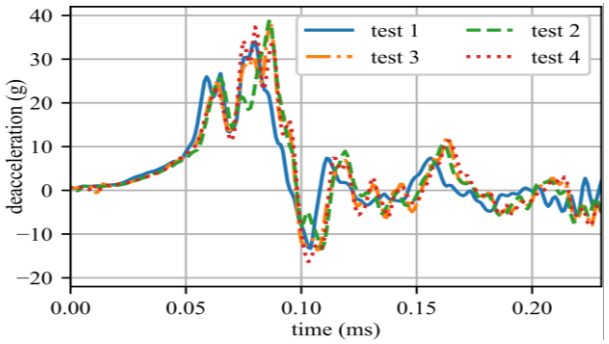
Ballistics packages

Vehicle collision

Blast protection damper

# HIGH-RATE DYNAMICS (CONTINUES)

- Goals:
  - Application: Real-time decision-making of structures
  - Required Technologies:
    - Low-latency model updating
    - System state prognostics in real-time
- Challenges:
  - Computing power is limited
    - memory, available energy, processors
  - Unknown sources of the inputs (forces, location)
  - Inability to calculate fault scenarios in advance
  - Rare and extreme situations



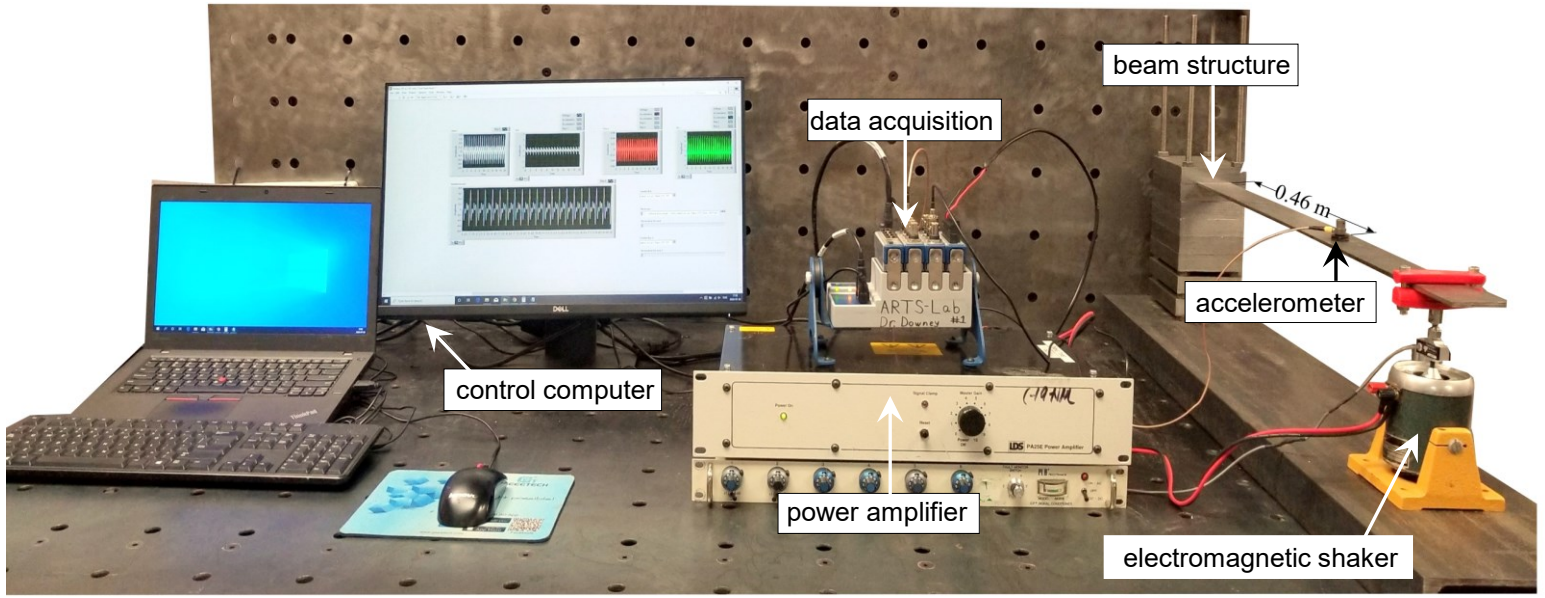
# METHODOLOGY

# CONTRIBUTIONS OF THIS WORK

- The development of an online structural vibration time series forecasting hardware/software system
- An experimental investigation showing the potential of the FFT-based time series forecasting methodology for high-rate signals
- A detailed discussion of the periodicity challenge for FFT-based time series forecasting
- The key focus for the current hardware implementation
    - FPGA resource utilization
    - timing constraints of various aspects of the methodology
    - algorithm accuracy and limitations concerning different data

# EXPERIMENTAL SETUP

# EXPERIMENTAL SETUP FOR DATA GENERATION

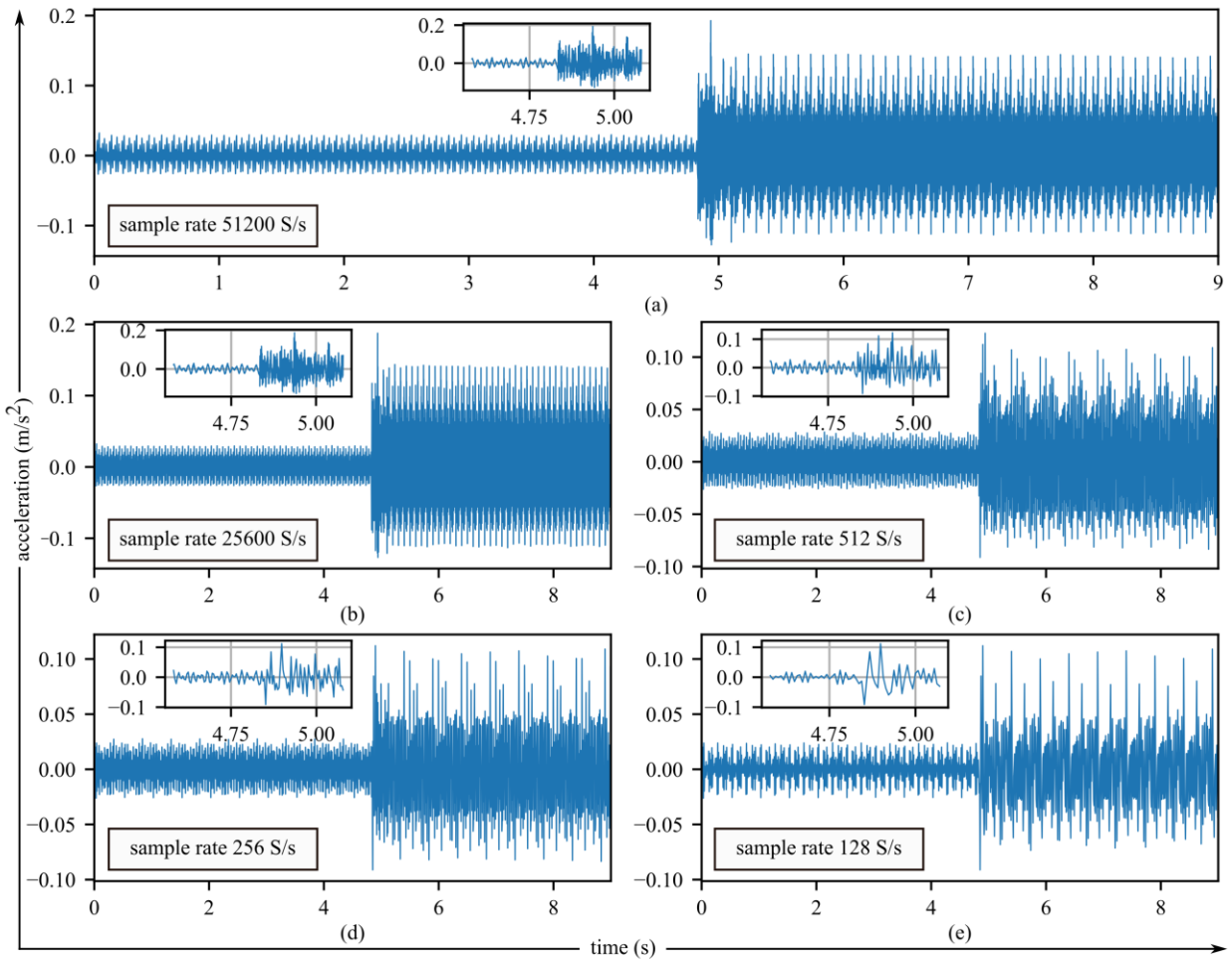



- This data is available in a public repository [1]

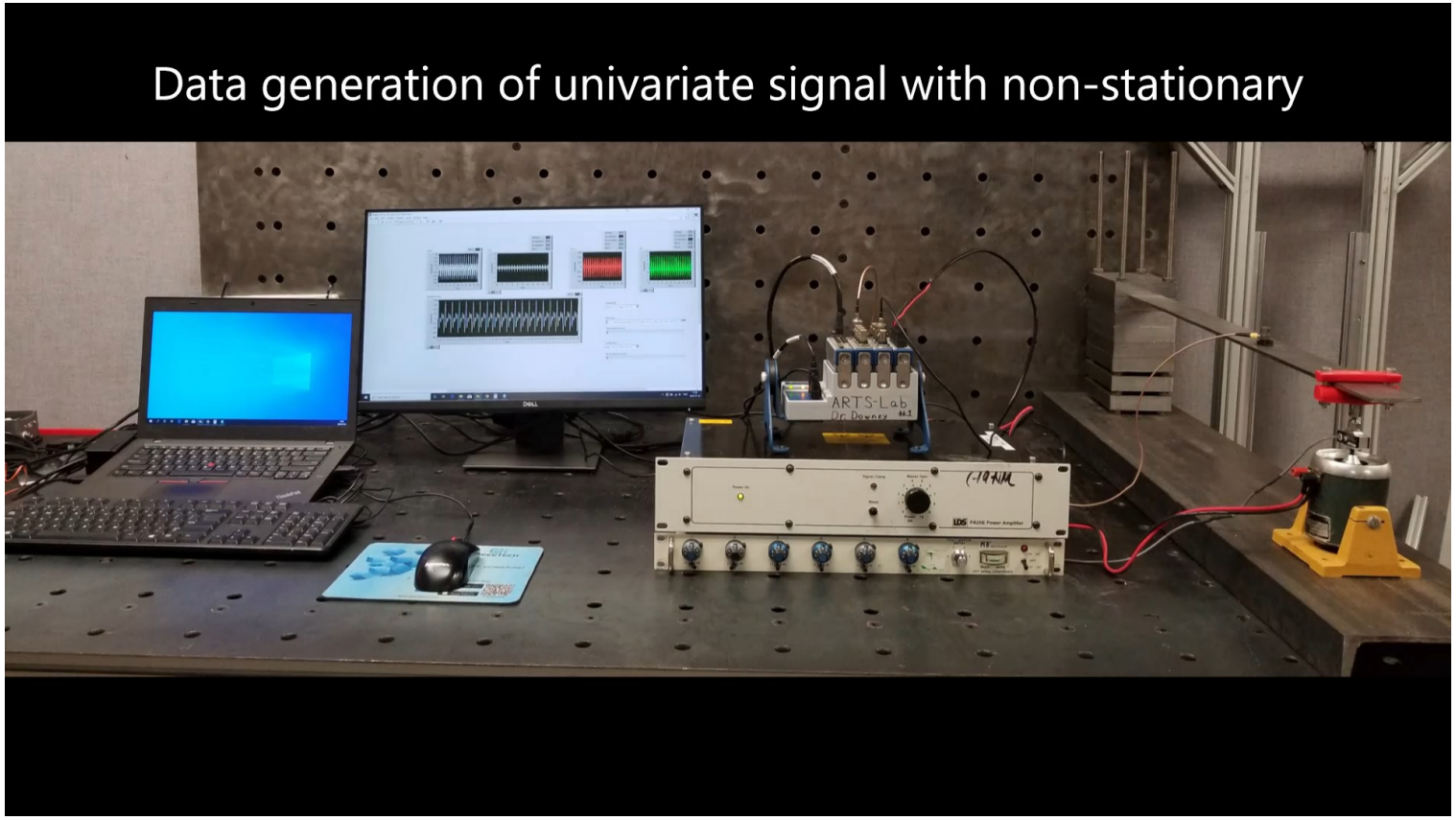
[1] High-Rate-SHM-Working-Group. Dataset-4 univariate signal with nonstationarity. https://github.com/High-RateSHM-Working-Group/Dataset-4-Univariate-signal-withnon-stationarity

# DATA STRUCTURE

- The structure's measured acceleration response for a composite sinusoidal input from the shaker.
- Two sine wave signals are concatenated together at *t*=5 where a nonstationary is present due to a change of frequency.
- The first half of the composite signal is built from 50, 70, and 100 Hz frequencies.
- The second half signal consists of 50 and 100 Hz frequencies.
- Four different sampled data were created from this data.

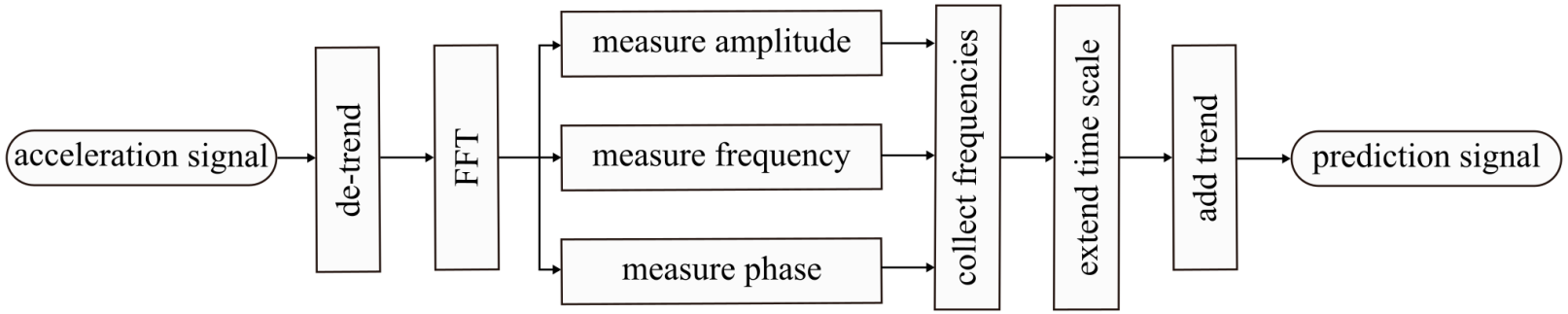


# DATA GENERATION EXPERIMENT VIDEO



# ALGORITHM

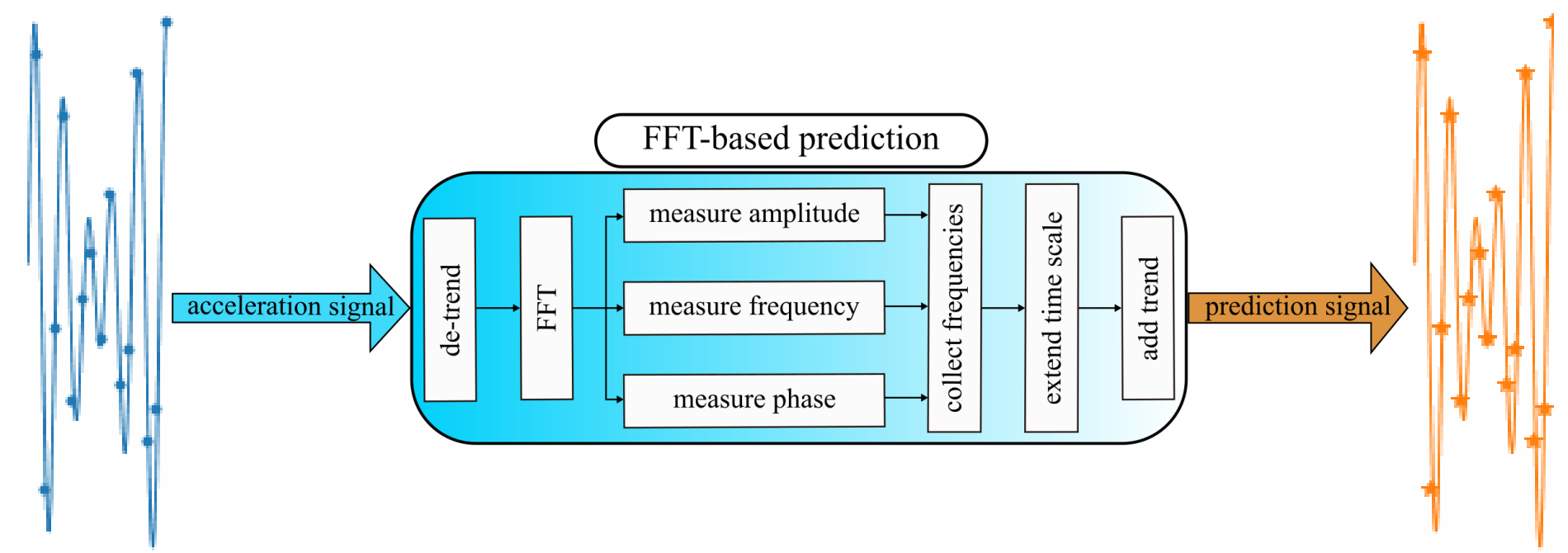
# ALGORITHM FOR FFT-BASED FORECASTING



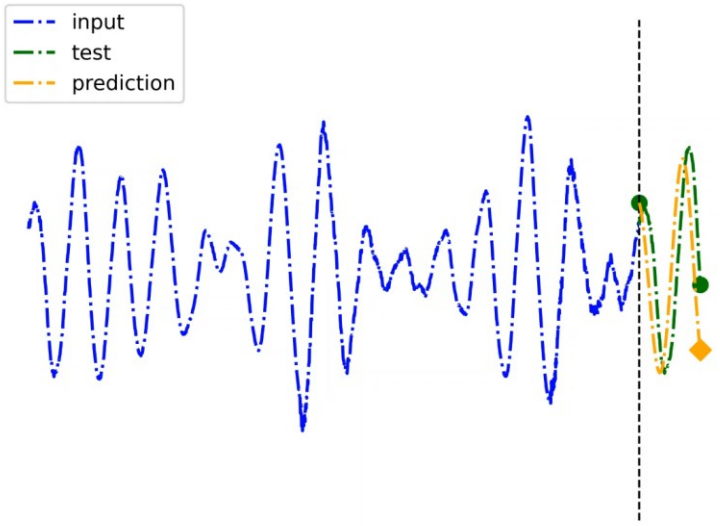

Schematic Algorithm diagram of FFT-based time series forecasting algorithms

- In FFT, the time domain and frequency domain maintain the circular topologies.
- The two endpoints of input length are assumed to meet at the same point.
- In a non-stationary signal, it is not possible to have all the embedded signals with different frequencies start at the same time.
- For accurately capturing all the frequencies, the minimum period should be higher than the Nyquist limit.

# ALGORITHM FOR FFT-BASED FORECASTING (CONTINUE)



# ALGORITHM FOR FFT-BASED FORECASTING (CONTINUE)



# PROBLEM STATEMENT

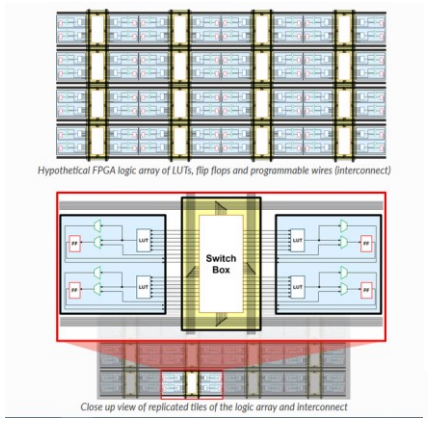
- The measured acceleration signal is
$$x_v = (x_1, x_2, x_3, \dots, x_v)$$
- The variable length sequence is
$$x_a = (x_{a1}, x_{a2}, x_{a3}, \dots, x_{aN})$$
- A polynomial function is used for finding trend.
$x_{trend} = p(x) = c_0 + c_1 x + c_2 x^2 + \cdots + cq^{x^q}$
- The new acceleration signal without trend is
$$x = x_a - x_{trend}$$
- As considered, the acceleration signal without the trend,
$$x = (x_1, x_2, x_3, \dots, x_N)$$


- The discrete Fourier transform (DFT) of that series
$$x_k = \sum_{n=0}^{N-1} x_n e^{(-i2\pi(kn/N))} \quad \text{for } k = 0, \dots, N$$
$$\omega = 2\pi/N = 2\pi f$$
$$(X_{amp})_k = |X_k|$$
$$(X_{phase})_k = X_k/|X_k|$$
- Similarly, the inverse DFT can be written as
$$x_n = \frac{1}{N} \sum_{k=0}^{N-1} x_k e^{(-i2\pi kn/N)} \quad \text{for } n = 0, \dots, N$$
- A new series of M length where M > N. The time series can be
$$x_m = \sum_{k=0}^{M-1} \left( (X_{amp})_k \cos\left(2\pi(\dot{k}\, m/M)\right) + (X_{phase})_k \right) \text{for } m = 1, \dots, M$$
- The time series with the trend information added back
$$x_{a\_new} = x_m + x_{trend}$$

# HARDWARE VALIDATION

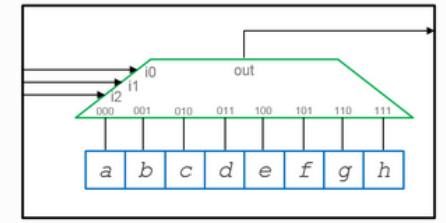
# INTRODUCTION TO FPGA

- FPGA: A field programmable gate array (FPGA)
  - A special kind of chip
  - Used in integrated circuit, silicon device, microchip, computer chip, or any designation compatible for programming
- CLB: A configurable logic block (CLB) is the basic
  - Repeating logic resource on an FPGA
  - contain smaller components, including flip-flops, look-up tables (LUTs), and multiplexers.
- Lookup Tables (LUTs):
  - A basic unit of computation at the heart of configurable logic in FPGAs
  - has a single bit output that is calculated based on the input signal values and the configurable table (or memory)
- Digital Signal Processing (DSP) Blocks:
  - Stratix® series FPGAs are an ideal solution for high-performance, high-precision DSP applications.
  - very power efficient and operate at far higher frequencies than the equivalent circuits in a soft implementation.
- Block RAMs:
  - Larger memories are also a significant resource on FPGAs
  - provide several kilobits of memory storage (Xilinx typically makes 18k or 36k available).

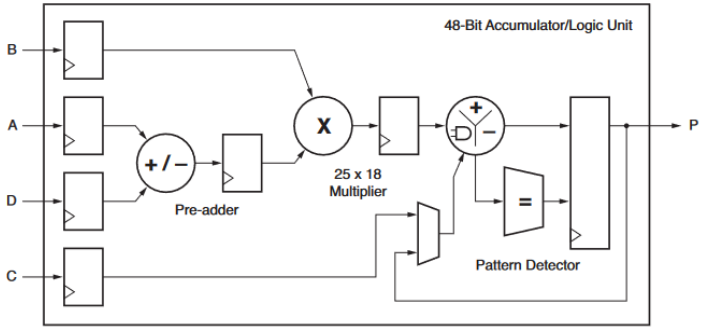



| i2 | i1 | i0 | out |
|---|---|---|---|
| 0 | 0 | 0 | a |
| 0 | 0 | 1 | b |
| 0 | 1 | 0 | c |
| 0 | 1 | 1 | d |
| 1 | 0 | 0 | e |
| 1 | 0 | 1 | f |
| 1 | 1 | 0 | g |
| 1 | 1 | 1 | h |

Truth table relationship of a LUT




LUT

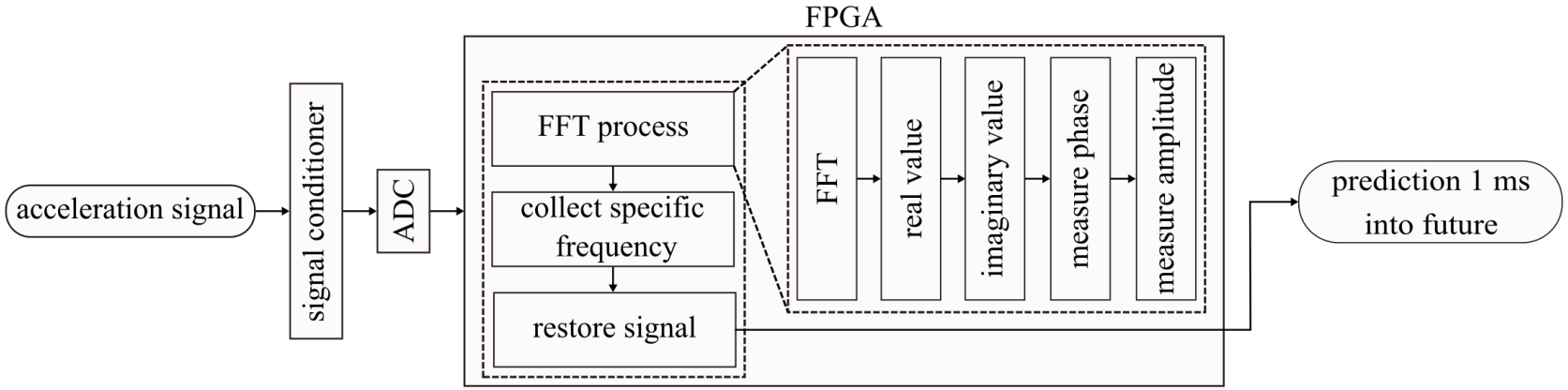



Basic DSP48E1 Slice Functionality



https://www.rapidwright.io/docs/FPGA_Architecture.html
https://www.xilinx.com/support/documentation/user_guides/ug479_7Series_DSP48E1.pdf
https://www.ni.com/documentation/en/labview-comms/latest/fpga-targets/configurable-logic-blocks/

# HARDWARE VALIDATION




Flowchart for data collection and processing during FFT-based forecasting in case of hardware implementation.

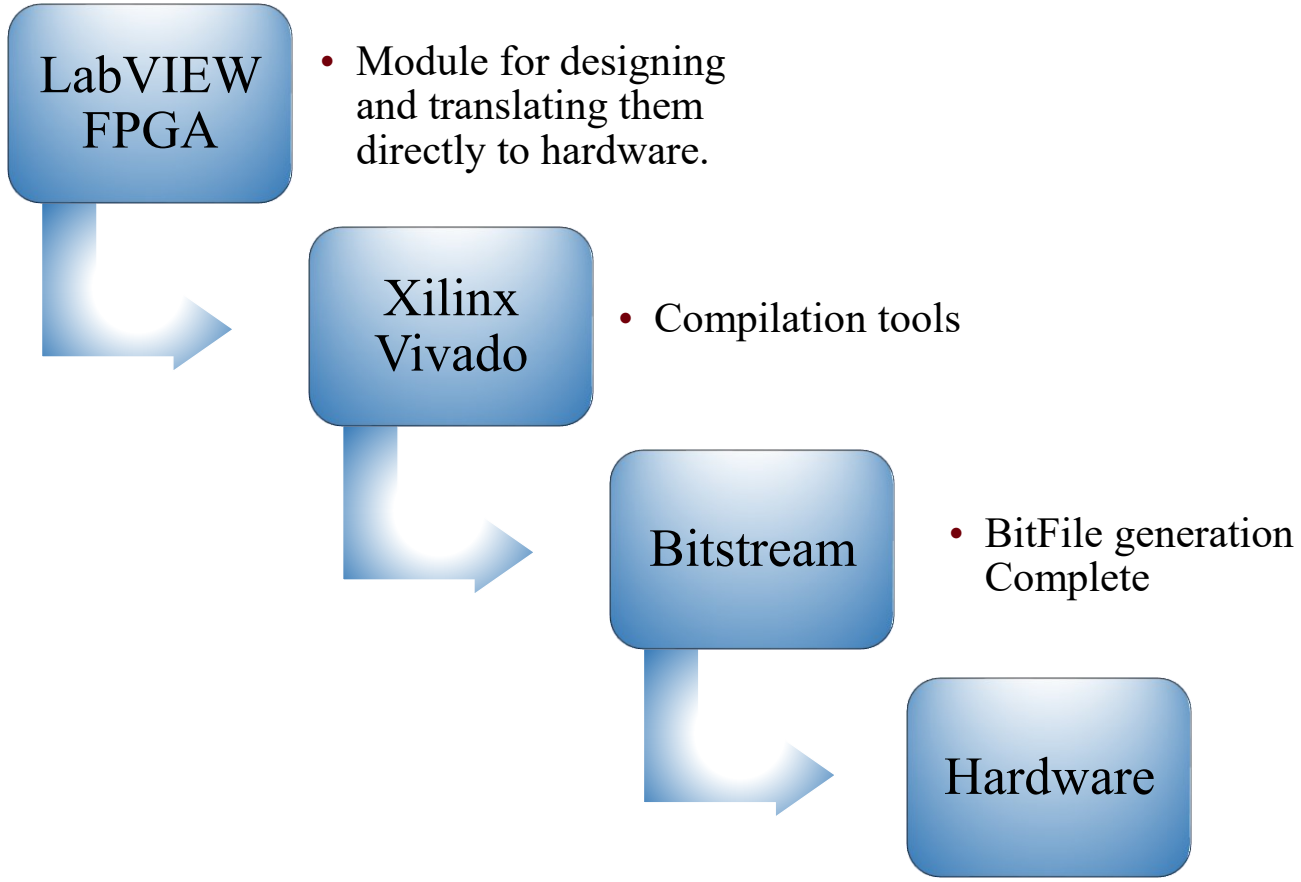
| sampling rate (S/s) | FFT size | input (samples) |
|---|---|---|
| 25600 | 128 | 256 |
| 512 | 512 | 512 |
| 256 | 256 | 256 |
| 128 | 128 | 128 |

# HARDWARE CONFIGURATION

- A Kintex-7 70T FPGA housed in a NI cRIO-9035
- incorporates a CPU running NI Linux Real-Time
- 1.33 GHz Dual-Core CPU
- 1 GB DRAM
- 4 GB Storage
- 8-Slot CompactRIO Controller
- The sampling rate of the hardware system is set from 128 to 51,200~S/s
- Internal clock of 24-bit ADC
- Data stored in the FPGA's look-up table memory
- The built-in LabVIEW FPGA FFT function has a range of size limitations between 8 to 8192 samples.
- Each size of FFT has a latency of cycles from 16 to 16384.


cRIO-9035
**Kintex-7 70T FPGA**

# FPGA WORKFLOW

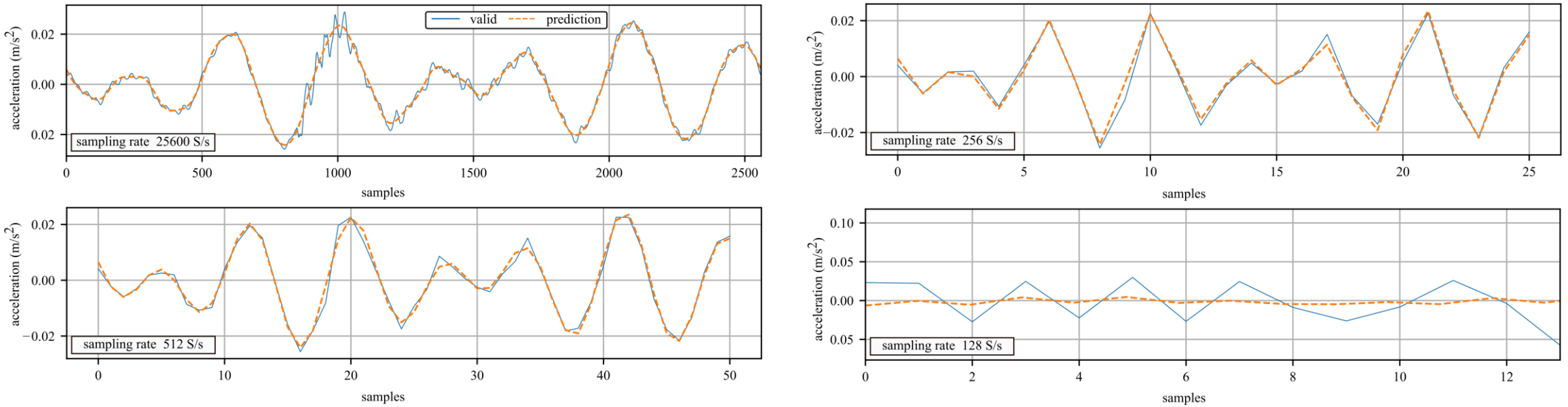



https://knowledge.ni.com/KnowledgeArticleDetails?id=kA03q000000YHVTCA4&l=en-US

# RESULTS AND DISCUSSION

# SIMULATION RESULTS

- Compared to the higher sampled data 25600 S/s, the prediction accuracy for the lowest sampled data, 128 S/s, is poor.



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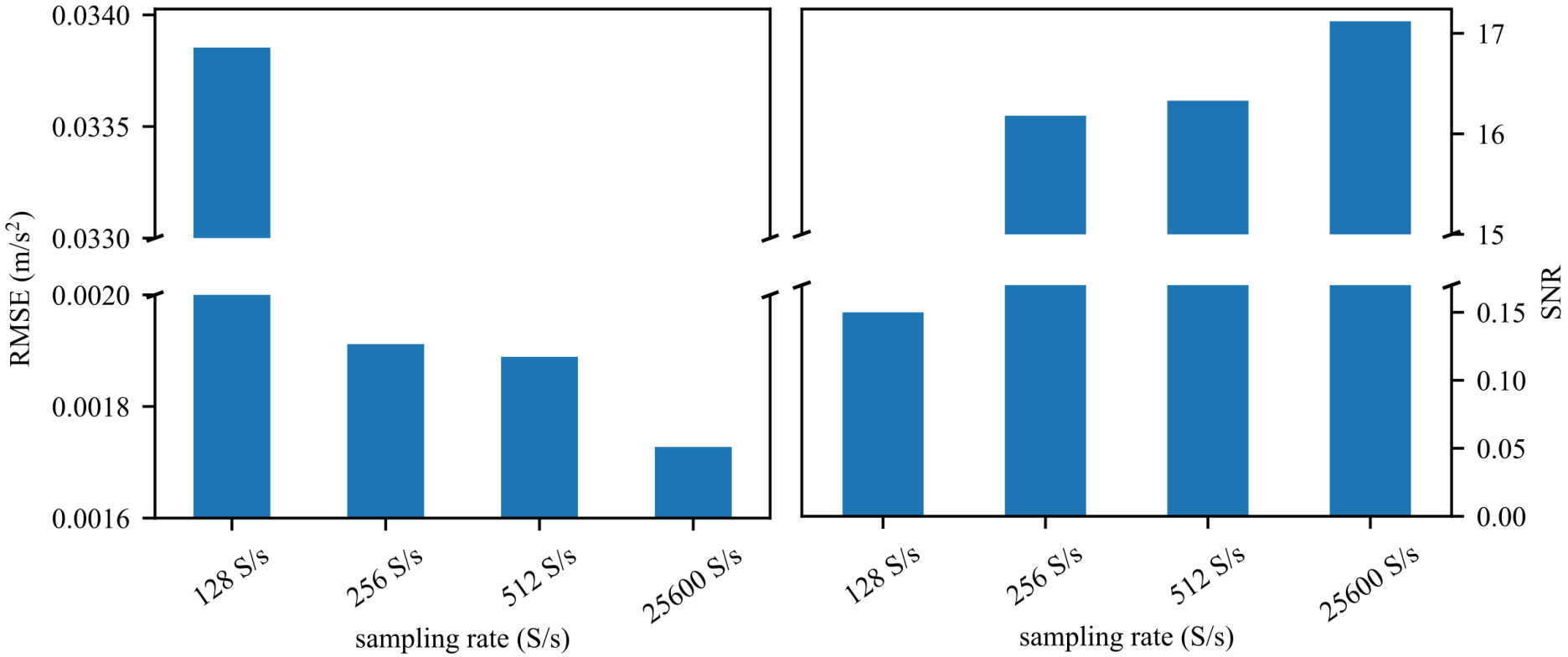
# SIMULATION RESULTS (CONTINUE)

- The frequency list reveals that 25600 S/s utilized more frequencies.

| Sample rate (S/s) | RMSE | SNR | frequency list |
|---|---|---|---|
| 25600 | 0.0017 | 17.12 | 50, 70, 100, 210, 220, 240, 260, 280, -50, -70, -100, -210,-220, -240, -260, -280 |
| 512 | 0.0019 | 16.33 | 50, 70, 100, -50, -70, -100 |
| 256 | 0.0019 | 16.18 | 50, 70, 100, -50, -70, -100 |
| 128 | 0.0338 | 0.15 | 50, 58, 22, 14, 20, 24, -50, -58, -22, -14, -20, -24 |

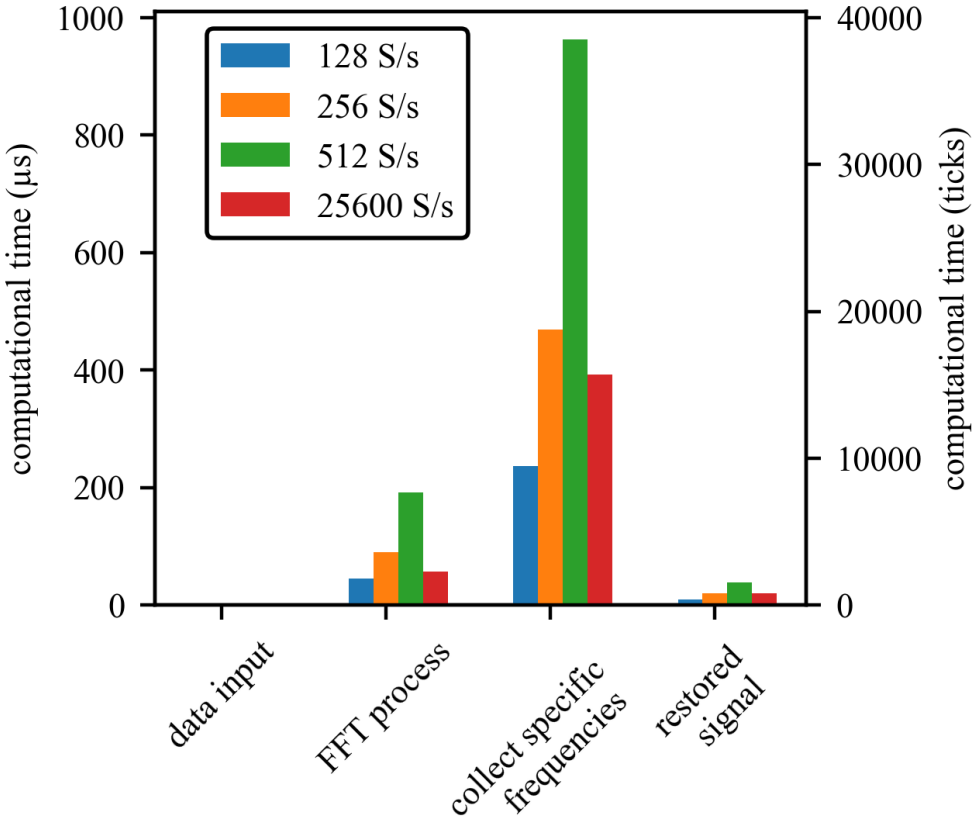


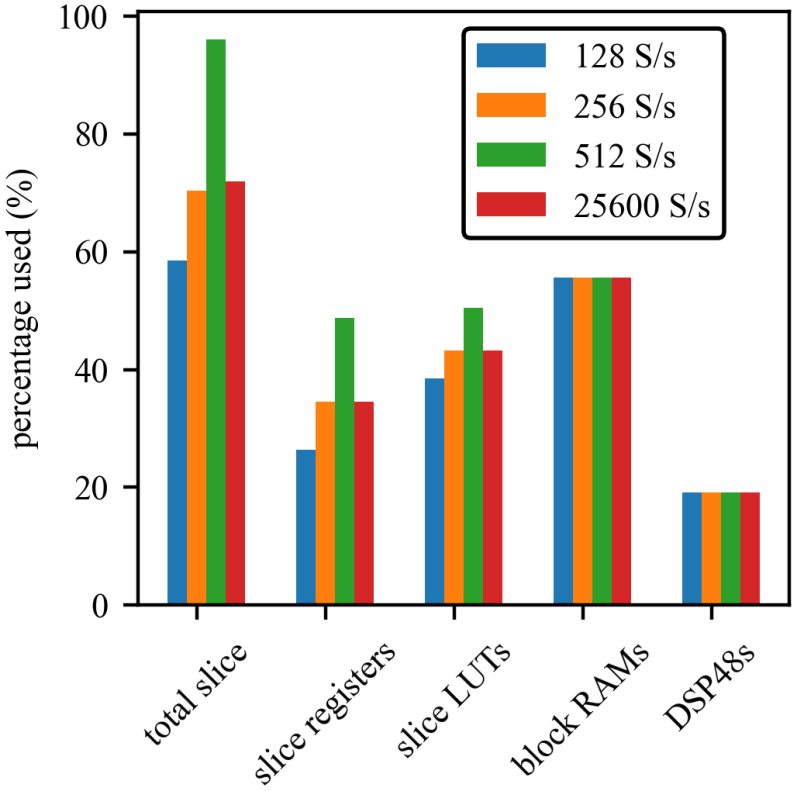



Carolina

# HARDWARE VALIDATION RESULTS

- The 512 S/s sampling rate takes greater computation time than other sampling rates.
- This is because the sample rate of 512 S/s is paired with an FFT size of 512; which maximizes the device hardware.
- Device utilization, the signal sampled at 512 S/s uses 96% of the FPGA slices.
- The 25600 S/s required its pairing with reduced FFT sizes to enable its deployment on the chosen FPGA hardware.



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# CONCLUSION

# CONCLUSION

- The current hardware (Kintex-7 70T), only data sampled at 512 S/s is viable for real-time time series forecasting of the considered system with a total system latency of 39.05 μs in restoring signal.
- A sampling speed of 25600 S/s requires FPGA resources beyond that provided by the chosen hardware.
- Future work will investigate the deployment of a hardware-in-a-loop implementation of the hardware/software system proposed here.

# ACKNOWLEDGEMENT

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# THANKS!